FORMFACTOR INC
Form S-1
October 20, 2003

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As filed with the Securities and Exchange Commission on October 17, 2003
Registration No. 333-

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

FORM S-1

REGISTRATION STATEMENT
Under
THE SECURITIES ACT OF 1933

FORMFACTOR, INC.

(Exact name of Registrant as specified in its charter)

Delaware	3825	13-3711155
(State or other jurisdiction of incorporation or organization)	(Primary standard industrial classification code number)	(I.R.S. employer identification no.)

FormFactor, Inc.

2140 Research Drive
Livermore, California 94550
(925) 294-4300
(Address, including zip code, and telephone number, including area code, of Registrant s principal executive offices)

Jens Meyerhoff

Chief Financial Officer and Senior Vice President of Operations
FormFactor, Inc.
2140 Research Drive
Livermore, California 94550
(925) 294-4300
(Name, address, including zip code, and telephone number, including area code, of agent for service)

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Approximate date of commencement of proposed sale to the public:

As soon as practicable after the effective date of this Registration Statement.

If any of the securities being registered on this form are to be offered on a delayed or continuous basis pursuant to Rule 415 under the Securities Act of 1933, check the following box. o _____

If this form is filed to register additional securities for an offering pursuant to Rule 462(b) under the Securities Act of 1933, check the following box and list the Securities Act registration statement number of the earlier effective registration statement for the same offering. o _____

If this form is a post-effective amendment filed pursuant to Rule 462(c) under the Securities Act of 1933, check the following box and list the Securities Act registration statement number of the earlier effective registration statement for the same offering. o _____

If this form is a post-effective amendment filed pursuant to Rule 462(d) under the Securities Act of 1933, check the following box and list the Securities Act registration statement number of the earlier effective registration statement for the same offering. o _____

If delivery of the prospectus is expected to be made pursuant to Rule 434 under the Securities Act of 1933, please check the following box. o _____

CALCULATION OF REGISTRATION FEE

Title of Each Class of Securities to be Registered	Amount to be Registered(1)	Proposed Maximum Offering Price Per Share(2)	Proposed Maximum Aggregate Offering Price(2)	Amount of Registration Fee(3)
Common stock, $.001 par value per share	5,750,000 shares	$25.52	$146,740,000	$11,871

(1) Includes 750,000 shares that the underwriters have the option to purchase to cover over-allotments, if any.

(2) Estimated solely for the purpose of computing the amount of the registration fee pursuant to Rule 457(c) under the Securities Act of 1933, and based on the average of the high and low prices of the common stock reported on the Nasdaq National Market on October 17, 2003.

(3) A fee of $7,214 was previously paid by the Registrant and such fee is credited against the registration fee for this Registration Statement pursuant to Rule 457 under the Securities Act of 1933.

The Registrant hereby amends this Registration Statement on such date or dates as may be necessary to delay the effective date of this Registration Statement until the Registrant shall file a further amendment that specifically states that this Registration Statement shall thereafter become effective in accordance with Section 8(a) of the Securities Act of 1933 or until this Registration Statement shall become effective on such date as the Securities and Exchange Commission, acting pursuant to said Section 8(a), may determine.

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The information in this prospectus is not complete and may be changed. We may not sell these securities until the registration statement filed with the Securities and Exchange Commission is effective. This prospectus is not an offer to sell these securities and we are not soliciting an offer to buy these securities in any jurisdiction where the offer or sale is not permitted.

PROSPECTUS (Subject to Completion)
Issued October 17, 2003

5,000,000 Shares

COMMON STOCK

FormFactor, Inc. is offering 1,499,866 shares of its common stock and the selling stockholders are offering 3,500,134 shares. FormFactor will not receive any of the proceeds from the sale of shares by the selling stockholders.

Our common stock is quoted on the Nasdaq National Market under the symbol FORM. The last reported sale price of our common stock on October 17, 2003 was $25.47 per share.

Investing in our common stock involves risks. See Risk Factors beginning on page 8.

PRICE $ A SHARE

	Price to Public	Underwriting Discounts and Commissions	Proceeds to FormFactor	Proceeds to Selling Stockholders
Per Share	*$*	*$*	*$*	*$*
Total	*$*	*$*	*$*	*$*

FormFactor, Inc. has granted the underwriters the right to purchase up to an additional 750,000 shares to cover over-allotments.

The Securities and Exchange Commission and state securities regulators have not approved or disapproved these securities, or determined if this prospectus is truthful or complete. Any representation to the contrary is a criminal offense.

Morgan Stanley & Co. Incorporated expects to deliver the shares to purchasers on , 2003.

MORGAN STANLEY

GOLDMAN, SACHS & CO.

, 2003

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You should rely only on the information contained in this prospectus. Neither we nor the selling stockholders have authorized anyone to provide you with information different from that contained in this prospectus. We and the selling stockholders are offering to sell, and seeking offers to buy, shares of our common stock only in jurisdictions where offers and sales are permitted. The information in this prospectus is accurate only as of the date of this prospectus, regardless of the time of delivery of this prospectus or of any sale of our common stock.

For investors outside the United States: Neither we, the selling stockholders nor any of the underwriters have done anything that would permit this offering, or possession or distribution of this prospectus in any jurisdiction where action for that purpose is required, other than in the United States. You are required to inform yourselves about and to observe any restrictions relating to this offering and the distribution of this prospectus.

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PROSPECTUS SUMMARY

You should read the following summary together with the entire prospectus, including the more detailed information in our consolidated financial statements and related notes appearing elsewhere in this prospectus. You should carefully consider, among other things, the matters discussed in Risk Factors.

FORMFACTOR, INC.

We design, develop, manufacture, sell and support precision, high performance advanced semiconductor wafer probe cards. In 2002, we were the leader in the advanced wafer probe card market in terms of revenues. Our products are based on our proprietary MicroSpring™ interconnect technology, which includes resilient spring-like contacts that we manufacture using precision micro-machining and scalable semiconductor-like wafer fabrication processes. Our technology enables us to produce wafer probe cards for test applications that require reliability, speed, precision and signal integrity.

The semiconductor industry has historically separated the manufacture of chips into two distinct parts: the front-end wafer fabrication process and the back-end assembly, packaging and final test process. Test is a critical and expensive part of semiconductor manufacturing and is performed in both the front-end and back-end processes. In the front-end, wafer probe test is performed on the whole wafer using wafer probe cards, and in the back-end, final test is performed on the individual packaged chip.

The semiconductor industry is experiencing a critical technology evolution driven by movement to smaller chip geometries, migration to 300 mm wafers, transition to copper interconnects and introduction of new insulating materials such as low-k and super low-k dielectrics. This evolution is pushing conventional wafer probe card technologies to their practical performance limits due to one or more factors, including: the inability to test in parallel many chips on a wafer; poor signal integrity; the inability to make precise contact with shrinking bond pad sizes and pitches; the inability to test accurately over a wide range of temperatures; and the inability to contact the wafer without damaging the chips on the wafer. While conventional wafer probe cards address some of these performance limitations, no conventional technology solves all of them.

Our MicroSpring interconnect technology and our proprietary design tools and technologies solve the limitations of conventional wafer probe cards by providing:

- a high degree of parallelism that enables our customers to test a significant number of chips at the same time in a single touchdown, which reduces total wafer test time and the overall cost of test;
- superior signal integrity, enabling customers to improve yields;
- micro-machining and semiconductor-like wafer fabrication processes that enable us to scale our products to shrinking semiconductor geometries;
- thermal compensation to permit wafer probe testing over a wide range of temperatures; and
- low contact force to permit testing without damage to the chips, particularly those incorporating fragile next-generation materials, such as low-k and super low-k dielectrics.

The current evolution of the semiconductor manufacturing process is driving a substantial increase in the cost of building new manufacturing capacity, with the cost of a leading edge 300 mm wafer manufacturing facility now approaching or exceeding $3.0 billion. With ever increasing capital investments, semiconductor manufacturers are focusing on ways to accelerate their return on investment by increasing volumes and yields, decreasing the overall costs of manufacturing and improving the time to market of their products. One area of focus is test because it provides vital feedback to the design and wafer fabrication processes.

In addition to addressing the shortcomings of conventional wafer probe cards, we believe that our customers will be able to use our technology to perform more advanced test functions on devices at the wafer-level in the front-end, rather than on individual devices in the back-end. This will enable them to optimize their manufacturing pipeline, from initial device design and fabrication through assembly, packaging and final test. As

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a result, manufacturers will be able to accelerate their return on investment by improving time to market, yield and volume.

Our objectives are to enhance our position as the leading supplier of advanced wafer probe card solutions and to apply our core MicroSpring interconnect technology to drive wafer-level economies of scale in semiconductor test. The principal elements of our strategy include: enhancing our market leadership in the dynamic random access memory, or DRAM, industry; expanding our presence in the flash memory market; increasing our penetration into the logic market; enabling migration of elements of final test to the wafer level; extending our technology leadership position; and continuing to build on our strategic relationships.

We introduced our first wafer probe card based on our MicroSpring interconnect technology in 1995, and, by the end of 2000, we were the leading supplier of advanced wafer probe cards, based on revenues. Our customers include the top 10 DRAM manufacturers, the world s largest microprocessor company, and four of the top 10 flash memory manufacturers, and, combined, these identified groups of our customers account for substantially all of our revenues. We focus our research and development activities on expanding our products into new markets and expanding applications for our MicroSpring interconnect technology. We manufacture our wafer probe cards in Livermore, California, and sell and support our products worldwide through our direct sales force, a distributor and independent sales representatives.

We were incorporated in Delaware in April 1993. Our principal executive offices are located at 2140 Research Drive, Livermore, California 94550, and our telephone number at that address is (925) 294-4300. Our Web site address is formfactor.com. The information on our Web site does not constitute part of this prospectus.

FormFactor, the FormFactor logo, MicroSpring, MicroForce, MicroLign and MOST are trademarks of FormFactor in the United States and other countries. All other trademarks, trade names or service marks appearing in this prospectus are the property of their respective owners.

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THE OFFERING

Common stock offered:	
By FormFactor	1,499,866 shares
By the selling stockholders	3,500,134 shares
Total	5,000,000 shares
Common stock to be outstanding after this offering	35,791,828 shares
Use of proceeds	We anticipate using the net proceeds to us from this offering for general corporate purposes and working capital requirements. We may also use a portion of the net proceeds to fund possible investments in, or acquisitions of, complementary businesses, products or technologies or establishing joint ventures. We will not receive any proceeds from the sale of common stock by the selling stockholders in this offering. See Use of Proceeds.
Nasdaq National Market symbol	FORM

The number of shares of our common stock to be outstanding immediately after this offering is based on 34,264,333 shares of our common stock outstanding on September 27, 2003. The number of shares of our common stock that will be outstanding immediately after this offering also includes 27,629 shares of common stock issuable upon exercise of options outstanding at September 27, 2003 with a weighted average exercise price of $5.71 per share. These options will be exercised by four selling stockholders, and the shares purchased through these exercises will be sold in this offering.

Unless otherwise indicated, all information in this prospectus assumes that the underwriters do not exercise their over-allotment option.

The number of shares of our common stock that will be outstanding immediately after this offering excludes:

7,050,111 shares of common stock issuable upon exercise of options outstanding at September 27, 2003 with a weighted average exercise price of $8.25 per share, which amount includes 27,629 shares of common stock subject to options that will be exercised by four selling stockholders in this offering. We have included the 27,629 shares in our calculation of our shares outstanding after this offering;

118,227 shares of common stock issuable upon exercise of warrants outstanding at September 27, 2003 with a weighted average exercise price of $5.25 per share;

2,210,881 shares of common stock available for issuance under our equity incentive plan at September 27, 2003; and

1,500,000 shares of common stock available for issuance under our employee stock purchase plan at September 27, 2003.

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SUMMARY CONSOLIDATED FINANCIAL DATA

The following tables provide summary consolidated financial data and should be read in conjunction with Management s Discussion and Analysis of Financial Condition and Results of Operations and our consolidated financial statements and the related notes appearing elsewhere in this prospectus.

	Fiscal Year Ended					Nine Months Ended	
	Dec. 26, 1998	Dec. 25, 1999	Dec. 30, 2000	Dec. 29, 2001	Dec. 28, 2002	Sept. 28, 2002	Sept. 27, 2003
							(unaudited)
	(in thousands, except per share data)						
Consolidated Statement of Operations Data:							
Revenues	$19,329	$35,722	$56,406	$73,433	$78,684	$56,527	$66,839
Cost of revenues	10,763	20,420	28,243	38,385	39,456	28,540	34,482
Gross margin	8,566	15,302	28,163	35,048	39,228	27,987	32,357
Total operating expenses	14,698	20,827	27,688	34,968	32,636	23,835	25,893
Operating income (loss)	(6,132)	(5,525)	475	80	6,592	4,152	6,464
Interest and other income (expense), net	157	(119)	1,719	477	642	404	780
Net income (loss)	$ (5,975)	$ (5,644)	$ 2,079	$ 250	$10,359	$ 8,770	$ 4,491
Net income (loss) per share:							
Basic	$ (3.60)	$ (2.16)	$ .61	$ .06	$ 2.33	$ 1.98	$ .27
Diluted	$ (3.60)	$ (2.16)	$ .08	$ .01	$ .35	$ .30	$ .14
Weighted-average number of shares used in per share calculations:							
Basic	1,659	2,609	3,408	4,029	4,448	4,436	16,669
Diluted	1,659	2,609	26,821	28,654	29,554	29,287	32,932

The as adjusted column of the consolidated balance sheet data reflects (i) the sale of 1,499,866 shares of common stock offered by us at an assumed public offering price of $25.47 per share, after deducting estimated underwriting discounts and commissions and estimated offering costs payable by us, and (ii) the proceeds from the exercise of options to purchase 27,629 shares of common stock by four selling stockholders in this offering.

	September 27, 2003	
	Actual	As Adjusted
	(unaudited) (in thousands)	
Consolidated Balance Sheet Data:		
Cash, cash equivalents and short-term investments	$101,084	$137,724
Working capital	110,465	147,105
Total assets	170,254	206,894
Deferred stock-based compensation, net	(12,007)	(12,007)
Total stockholders equity	150,444	187,084

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RISK FACTORS

Investing in our common stock involves a high degree of risk. You should carefully consider the following risk factors, as well as the other information in this prospectus, before deciding whether to invest in shares of our common stock. If any of the following risks actually occurs, our business, financial condition and results of operations would suffer. In this case, the trading price of our common stock would likely decline and you might lose all or part of your investment in our common stock. The risks described below are not the only ones we face. Additional risks that we currently do not know about or that we currently believe to be immaterial may also impair our business operations.

Risks Related to Our Business and Industry

Our operating results are likely to fluctuate, which could cause us to miss expectations about these results and cause the trading price of our common stock to decline.

Our operating results are likely to fluctuate. As a result, we believe that you should not rely on period-to-period comparisons of our financial results as an indication of our future performance. Factors that are likely to cause our revenues and operating results to fluctuate include those discussed in the risk factors below. If our revenues or operating results fall below the expectations of market analysts or investors, the market price of our common stock could decline substantially.

Cyclicality in the semiconductor industry historically has affected our sales and might do so in the future, and as a result we could experience reduced revenues or operating results.

The semiconductor industry has historically been cyclical and is characterized by wide fluctuations in product supply and demand. From time to time, this industry has experienced significant downturns, often in connection with, or in anticipation of, maturing product and technology cycles, excess inventories and declines in general economic conditions. This cyclicality could cause our operating results to decline dramatically from one period to the next. For example, our revenues in the three months ended September 29, 2001 declined by 25.5% compared to our revenues in the three months ended June 30, 2001, and our revenues in the three months ended March 29, 2003 declined by 15.7% compared to our revenues in the three months ended December 28, 2002. Our business depends heavily upon the development of new semiconductors and semiconductor designs, the volume of production by semiconductor manufacturers and the overall financial strength of our customers, which, in turn, depend upon the current and anticipated market demand for semiconductors and products, such as personal computers, that use semiconductors. Semiconductor manufacturers generally sharply curtail their spending during industry downturns and historically have lowered their spending disproportionately more than the decline in their revenues. As a result, if we are unable to adjust our levels of manufacturing and human resources or manage our costs and deliveries from suppliers in response to lower spending by semiconductor manufacturers, our gross margin might decline and cause us to experience operating losses.

If we do not keep pace with technological developments in the semiconductor industry, our products might not be competitive and our revenues and operating results could suffer.

We must continue to invest in research and development to improve our competitive position and to meet the needs of our customers. Our future growth depends, in significant part, upon our ability to work effectively with and anticipate the testing needs of our customers, and on our ability to develop and support new products and product enhancements to meet these needs on a timely and cost-effective basis. Our customers testing needs are becoming more challenging as the semiconductor industry continues to experience rapid technological change driven by the demand for complex circuits that are shrinking in size and at the same time are increasing in speed and functionality and becoming less expensive to produce. Examples of recent trends driving demand for technological research and development include semiconductor manufacturers transitions to 110 nanometer and 90 nanometer technology nodes, to 512 megabit density devices and to Double Date Rate II, or DDR II, architecture devices. Our customers expect that they will be able to integrate our wafer probe cards into any manufacturing process as soon as it is deployed. Therefore, to meet these expectations and remain competitive, we must continually design, develop and introduce on a timely basis new products and product enhancements

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with improved features. Successful product design, development and introduction on a timely basis require that we:

design innovative and performance-enhancing features that differentiate our products from those of our competitors;

transition our products to new manufacturing technologies;

identify emerging technological trends in our target markets;

maintain effective marketing strategies;

respond effectively to technological changes or product announcements by others; and

adjust to changing market conditions quickly and cost-effectively.

We must devote significant research and development resources to keep up with the rapidly evolving technologies used in semiconductor manufacturing processes. Not only do we need the technical expertise to implement the changes necessary to keep our technologies current, but we must also rely heavily on the judgment of our management to anticipate future market trends. If we are unable to timely predict industry changes, or if we are unable to modify our products on a timely basis, we might lose customers or market share. In addition, we might not be able to recover our research and development expenditures, which could harm our operating results.

If semiconductor memory device manufacturers do not convert to 300 mm wafers, our growth could be impeded.

The growth of our business for the foreseeable future depends in large part upon sales of our wafer probe cards to manufacturers of dynamic random access memory, or DRAM, and flash memory devices. The recent downturn in the semiconductor industry caused various chip manufacturers to readdress their respective strategies for converting existing 200 mm wafer fabrication facilities to 300 mm wafer fabrication, or for building new 300 mm wafer fabrication facilities. Some manufacturers have delayed, cancelled or postponed previously announced plans to convert to 300 mm wafer fabrication. We believe that the decision to convert to a 300 mm wafer fabrication facility is made by each manufacturer based upon both internal and external factors, such as:

current and projected chip prices;

projected price erosion for the manufacturer s particular chips;

supply and demand issues;

overall manufacturing capability within the manufacturer s target market(s);

the availability of funds to the manufacturer;

the technology roadmap of the manufacturer; and

the price and availability of equipment needed within the 300 mm facility.

One or more of these internal and external factors, as well as other factors, including factors that a manufacturer may choose to not publicly disclose, can impact the decision to maintain a 300 mm conversion schedule, to delay the conversion schedule for a period of time, or to cancel the conversion. It is also possible that the conversion to 300 mm wafers will occur on different schedules for DRAM chip manufacturers and flash memory chip manufacturers. We have invested significant resources to develop technology that addresses the market for 300 mm wafers. If manufacturers of memory devices delay or discontinue the transition to 300 mm wafers, or make the transition more slowly than we currently expect, our growth and profitability could be impeded. In addition, any delay in large-scale adoption of manufacturing based upon 300 mm wafers would provide time for other companies to develop and market products that compete with ours, which could harm our competitive position.

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We are subject to general economic and market conditions.

Our business is subject to the effects of general economic conditions in the United States and worldwide, and to market conditions in the semiconductor industry in particular. For example, in fiscal 2001, our operating results were adversely affected by unfavorable global economic conditions and reduced capital spending by semiconductor manufacturers. These adverse conditions resulted in a decrease in the demand for semiconductors and products using semiconductors, and in a sharp reduction in the development of new semiconductors and semiconductor designs. As a result, we experienced a decrease in the demand for our wafer probe cards. If the economic conditions in the United States and worldwide do not improve, or if they worsen from current levels, we could experience material negative effects on our business.

We depend upon the sale of our wafer probe cards for substantially all of our revenues, and a downturn in demand for our products could have a more disproportionate impact on our revenues than if we derived revenues from a more diversified product offering.

Historically, we have derived substantially all of our revenues from the sale of our wafer probe cards. We anticipate that sales of our wafer probe cards will represent a substantial majority of our revenues for the foreseeable future. Our business depends in large part upon continued demand in current markets for, and adoption in new markets of, current and future generations of our wafer probe cards. Large-scale market adoption depends upon our ability to increase customer awareness of the benefits of our wafer probe cards and to prove their reliability, ability to increase yields and cost effectiveness. We may be unable to sell our wafer probe cards to certain potential customers unless those customers change their device test strategies, change their wafer probe card and capital equipment buying strategies, or change or upgrade their existing test equipment. We might not be able to sustain or increase our revenues from sales of our wafer probe cards, particularly if conditions in the semiconductor market deteriorate or do not improve or if the market enters into another downturn in the future. Any decrease in revenues from sales of our wafer probe cards could harm our business more than it would if we offered a more diversified line of products.

If demand for our products in the memory device and flip chip logic markets declines or fails to grow as we anticipate, our revenues could decline.

We derive substantially all of our revenues from wafer probe cards that we sell to manufacturers of DRAM memory and flash memory devices and manufacturers of microprocessor, chipset and other logic devices. In the microprocessor, chipset and other logic device markets, our products are primarily used for devices employing flip chip packaging, which devices are commonly referred to as flip chip logic devices. In the nine months ended September 27, 2003, sales to manufacturers of DRAM devices accounted for 58.0% of our revenues, sales to manufacturers of flip chip logic devices accounted for 20.3% of our revenues, and sales to manufacturers of flash memory devices accounted for 21.1% of our revenues. For fiscal 2002, sales to manufacturers of DRAM devices accounted for 69.6% of our revenues, sales to manufacturers of flip chip logic devices accounted for 17.4% of our revenues, and sales to manufacturers of flash memory devices accounted for 11.7% of our revenues. Therefore, our success depends in part upon the continued acceptance of our products within these markets and our ability to continue to develop and introduce new products on a timely basis for these markets. For example, the market might not accept an increasingly high parallelism wafer test solution.

A substantial portion of these semiconductor devices is sold to manufacturers of personal computers and computer-related products. The personal computer market has historically been characterized by significant fluctuations in demand and continuous efforts to reduce costs, which in turn have affected the demand for and price of DRAM devices and microprocessors. The personal computer market might not grow in the future at historical rates or at all and design activity in the personal computer market might decrease, which could negatively affect our revenues and operating results.

The markets in which we participate are intensely competitive, and if we do not compete effectively, our operating results could be harmed.

The wafer probe card market is highly competitive. With the introduction of new technologies and market entrants, we expect competition to intensify in the future. In the past, increased competition has resulted in price

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reductions, reduced gross margins or loss of market share, and could do so in the future. Competitors might introduce new competitive products for the same markets that our products currently serve. These products may have better performance, lower prices and broader acceptance than our products. In addition, for products such as wafer probe cards, semiconductor manufacturers typically qualify more than one source, to avoid dependence on a single source of supply. As a result, our customers will likely purchase products from our competitors. Current and potential competitors include AMST Co., Ltd., Cascade Microtech, Inc., ESJ Corporation, Feinmetall GmbH, Japan Electronic Materials Corporation, Kulicke and Soffa Industries, Inc., Micronics Japan Co., Ltd., MicroProbe, Inc., NanoNexus Inc., Phicom Corporation, SCS Hightech, Inc., Tokyo Cathode Laboratory Co., Ltd. and Wentworth Laboratories, Inc., among others. Many of our current and potential competitors have greater name recognition, larger customer bases, more established customer relationships or greater financial, technical, manufacturing, marketing and other resources than we do. As a result, they might be able to respond more quickly to new or emerging technologies and changes in customer requirements, devote greater resources to the development, promotion, sale and support of their products, and reduce prices to increase market share. Some of our competitors also supply other types of test equipment, or offer both advanced wafer probe cards and needle probe cards. Those competitors that offer both advanced wafer probe cards and needle probe cards might have strong, existing relationships with our customers or with potential customers. Because we do not offer a needle probe card or other conventional technology wafer probe card for less advanced applications, it may be difficult for us to introduce our advanced wafer probe cards to these customers and potential customers for certain wafer test applications. It is possible that existing or new competitors, including test equipment manufacturers, may offer new technologies that reduce the value of our wafer probe cards. The wafer probe card market has historically been fragmented with many local suppliers serving individual customers.

However, recent consolidation has reduced the number of competitors. For example, in late 2000, Kulicke and Soffa Industries, Inc. acquired Probe Technology Corporation and Cerprobe Corporation. These and other combinations might result in a competitor gaining a significant advantage over us by enabling it to expand its product offerings and service capabilities to meet a broader range of customer needs.

We derive a substantial portion of our revenues from a small number of customers, and our revenues could decline significantly if any major customer cancels, reduces or delays a purchase of our products.

A relatively small number of customers has accounted for a significant portion of our revenues in any particular period. In the nine months ended September 27, 2003, four customers accounted for 69.6% of our revenues. In fiscal 2002, four customers accounted for 77.2% of our revenues. Our ten largest customers accounted for 94.9% of our revenues in the nine months ended September 27, 2003 and 97.4% of our revenues in fiscal 2002. We anticipate that sales of our products to a relatively small number of customers will continue to account for a significant portion of our revenues. The cancellation or deferral of even a small number of purchases of our products could cause our revenues to decline in any particular quarter. A number of factors could cause customers to cancel or defer orders, including manufacturing delays, interruptions to our customers operations due to fire, natural disasters or other events or a downturn in the semiconductor industry. Our agreements with our customers do not contain minimum purchase commitments, and our customers could cease purchasing our products with short or no notice to us or fail to pay all or part of an invoice. In some situations, our customers might be able to cancel orders without a significant penalty. In addition, the continuing trend toward consolidation in the semiconductor industry, particularly among manufacturers of DRAMs, could reduce our customer base and lead to lost or delayed sales and reduced demand for our wafer probe cards. Industry consolidation also could result in pricing pressures as larger DRAM manufacturers could have sufficient bargaining power to demand reduced prices and favorable nonstandard terms. Additionally, certain customers may not want to rely entirely or substantially on a single wafer probe card supplier and, as a result, such customers could reduce their purchases of our wafer probe cards.

If our relationships with our customers and companies that manufacture semiconductor test equipment deteriorate, our product development activities could be harmed.

The success of our product development efforts depends upon our ability to anticipate market trends and to collaborate closely with our customers and with companies that manufacture semiconductor test equipment. Our

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relationships with these customers and companies provide us with access to valuable information regarding manufacturing and process technology trends in the semiconductor industry, which enables us to better plan our product development activities. These relationships also provide us with opportunities to understand the performance and functionality requirements of our customers, which improve our ability to customize our products to fulfill their needs. Our relationships with test equipment companies are important to us because test equipment companies can design our wafer probe cards into their equipment and provide us with the insight into their product plans that allows us to offer wafer probe cards for use with their products when they are introduced to the market. Our relationships with our customers and test equipment companies could deteriorate if they:

become concerned about our ability to protect their intellectual property;

develop their own solutions to address the need for testing improvement;

regard us as a competitor;

establish relationships with others in our industry; or

attempt to restrict our ability to enter into relationships with their competitors.

Many of our customers and the test equipment companies we work with are large companies. The consequences of a deterioration in our relationship with any of these companies could be exacerbated due to the significant influence these companies can exert in our markets. If our current relationships with our customers and test equipment companies deteriorate, or if we are unable to develop similar collaborative relationships with important customers and test equipment companies in the future, our long-term ability to produce commercially successful products could be impaired.

Because we generally do not have a sufficient backlog of unfilled orders to meet our quarterly revenue targets, revenues in any quarter are substantially dependent upon customer orders received and fulfilled in that quarter.

Our revenues are difficult to forecast because we generally do not have a sufficient backlog of unfilled orders to meet our quarterly revenue targets at the beginning of a quarter. Rather, a majority of our revenues in any quarter depends upon customer orders for our wafer probe cards that we receive and fulfill in that quarter. Because our expense levels are based in part on our expectations as to future revenues and to a large extent are fixed in the short term, we might be unable to adjust spending in time to compensate for any unexpected shortfall in revenues. Accordingly, any significant shortfall of revenues in relation to our expectations could hurt our operating results.

We rely upon a distributor for a substantial portion of our revenues, and a disruption in our relationship with our distributor could have a negative impact on our revenues.

We rely on Spirox Corporation, our distributor in Taiwan, Singapore and China, for a substantial portion of our revenues. Sales to Spirox accounted for 15.1% of our revenues in the nine months ended September 27, 2003 and 20.9% of our revenues in fiscal 2002. Spirox also provides customer support. A reduction in the sales or service efforts or financial viability of our distributor, or deterioration in, or termination of, our relationship with our distributor could harm our revenues, our operating results and our ability to support our customers in the distributor s territory. In addition, establishing alternative sales channels in the region could consume substantial time and resources, decrease our revenues and increase our expenses.

If our relationships with our independent sales representatives change, our business could be harmed.

We currently rely on independent sales representatives to assist us in the sale of our products in various geographic regions. If we make the business decision to terminate or modify our relationships with one or more of our independent sales representatives, or if an independent sales representative decides to disengage from us, and we do not effectively and efficiently manage such a change, we could lose sales to existing customers and fail to obtain new customers.

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If semiconductor manufacturers do not migrate elements of final test to wafer probe test, market acceptance of other applications of our technology could be delayed.

We intend to work with our customers to migrate elements of final test from the device level to the wafer level. This migration will involve a change in semiconductor test strategies from concentrating final test at the individual device level to increasing the amount of test at the wafer level. Semiconductor manufacturers typically take time to qualify new strategies that affect their testing operations. As a result, general acceptance of wafer-level final test might not occur in the near term or at all. In addition, semiconductor manufacturers might not accept and use wafer-level final test in a way that uses our technology. If the migration of elements of final test to wafer probe test does not grow as we anticipate, or if semiconductor manufacturers do not adopt our technology for their wafer probe test requirements, market acceptance of other applications for our technology could be delayed.

Changes in test strategies, equipment and processes could cause us to lose revenues.

The demand for wafer probe cards depends in large part upon the number of semiconductor designs and the overall semiconductor unit volume. The time it takes to test a wafer depends upon the number of devices being tested, the complexity of these devices, the test software program and the test equipment itself. As test programs become increasingly effective and test throughput increases, the number of wafer probe cards required to test a given volume of devices declines. Therefore, advances in the test process could cause us to lose sales.

If semiconductor manufacturers implement chip designs that include built-in self-test capabilities, or similar functions or methodologies that increase test throughput, it could negatively impact our sales or the migration of elements of final test to the wafer level. Additionally, if new chip designs or types of chips are implemented that require less, or even no, test using wafer probe cards, our revenues could be impacted. Further, if new chip designs are implemented which we are unable to test, or which we are unable to test efficiently and provide our customers with an acceptably low overall cost of test, our revenues could be negatively impacted.

We incur significant research and development expenses in conjunction with the introduction of new product platforms. Often, we time our product introductions to the introduction of new test equipment platforms. Because our customers require both test equipment and wafer probe cards, any delay or disruption of the introduction of new test equipment platforms would negatively affect our growth.

We manufacture all of our products at a single facility, and any disruption in the operations of that facility could adversely impact our business and operating results.

Our processes for manufacturing our wafer probe cards require sophisticated and costly equipment and a specially designed facility, including a semiconductor clean room. We manufacture all of our wafer probe cards at one facility located in Livermore, California. Any disruption in the operation of that facility, whether due to technical or labor difficulties, destruction or damage from fire or earthquake, infrastructure failures such as power or water shortage or any other reason, could interrupt our manufacturing operations, impair critical systems, disrupt communications with our customers and suppliers and cause us to write off inventory and to lose sales. In addition, if the recent energy crises in California that resulted in disruptions in power supply and increases in utility costs were to recur, we might experience power interruptions and shortages, which could disrupt our manufacturing operations. This could subject us to loss of revenues as well as significantly higher costs of energy. Further, current and potential customers might not purchase our products if they perceive our lack of an alternate manufacturing facility to be a risk to their continuing source of supply.

The transition to our new manufacturing facilities could cause a decline in our operating results.

We plan to move our manufacturing operations into a new facility in Livermore in 2004. The costs of starting up our new manufacturing facility, including capital costs such as equipment and fixed costs such as rent, will be substantial. We might not be able to shift from our current production facility to the new production facility efficiently or effectively. The transition will require us to have both our existing and new manufacturing facilities operational for several quarters. This will cause us to incur significant costs due to redundancy of infrastructure at both sites. Furthermore, the qualification of the new manufacturing facility will require us to use

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materials and build product and product components that will not be sold to our customers, causing higher than normal material spending. The transition might also lead to manufacturing interruptions, which could mean delayed deliveries or lost sales. Some or all of our customers could require a full qualification of our new facility. Any qualification process could take longer than we anticipate. Any difficulties with the transition or with bringing the new manufacturing facility to full capacity and volume production could increase our costs, disrupt our production process and cause delays in product delivery and lost sales, which would harm our operating results.

If we are unable to manufacture our products efficiently, our operating results could suffer.

We must continuously modify our manufacturing processes in an effort to improve yields and product performance, lower our costs and reduce the time it takes us to design and produce our products. We will incur significant start-up costs associated with implementing new manufacturing technologies, methods and processes and purchasing new equipment, which could negatively impact our gross margin. We could experience manufacturing delays and inefficiencies as we refine new manufacturing technologies, methods and processes, implement them in volume production and qualify them with customers, which could cause our operating results to decline. The risk of encountering delays or difficulties increases as we manufacture more complex products. In addition, if demand for our products increases, we will need to expand our operations to manufacture sufficient quantities of products without increasing our production times or our unit costs. As a result of such expansion, we could be required to purchase new equipment, upgrade existing equipment, develop and implement new manufacturing processes and hire additional technical personnel. Further, new or expanded manufacturing facilities could be subject to qualification by our customers. In the past, we have experienced difficulties in expanding our operations to manufacture our products in volume on time and at acceptable cost. Any difficulties in expanding our manufacturing operations could cause product delivery delays and lost sales. If demand for our products decreases, we could have excess manufacturing capacity. The fixed costs associated with excess manufacturing capacity could cause our operating results to decline. If we are unable to achieve further manufacturing efficiencies and cost reductions, particularly if we are experiencing pricing pressures in the marketplace, our operating results could suffer.

If we are unable to continue to reduce the time it takes for us to design and produce a wafer probe card, our growth could be impeded.

Our customers continuously seek to reduce the time it takes them to introduce new products to market. The cyclicality of the semiconductor industry, coupled with changing demands for semiconductor devices, requires our customers to be flexible and highly adaptable to changes in the volume and mix of products they must produce. Each of those changes requires a new design and each new design requires a new wafer probe card. For some existing semiconductor devices, the manufacturers volume and mix of product requirements are such that we are unable to design, manufacture and ship products to meet such manufacturers relatively short cycle time requirements. If we are unable to reduce the time it takes for us to design, manufacture and ship our products in response to the needs of our customers, our competitive position could be harmed. If we are unable to meet a customer s schedule for wafer probe cards for a particular design, our customer might purchase wafer probe cards from a competitor and we might lose sales.

We obtain some of the components and materials we use in our products from a single or sole source or a limited group of suppliers, and the partial or complete loss of one of these suppliers could cause production delays and a substantial loss of revenues.

We obtain some of the components and materials used in our products, such as printed circuit board assemblies, plating materials and ceramic substrates, from a single or sole source or a limited group of suppliers. Alternative sources are not currently available for sole source components and materials. Because we rely on purchase orders rather than long-term contracts with the majority of our suppliers, we cannot predict with certainty our ability to obtain components and materials in the longer term. A sole or limited source supplier could increase prices, which could lead to a decline in our gross margin. Our dependence upon sole or limited source suppliers exposes us to several other risks, including a potential inability to obtain an adequate supply of

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materials, late deliveries and poor component quality. Disruption or termination of the supply of components or materials could delay shipments of our products, damage our customer relationships and reduce our revenues. For example, if we were unable to obtain an adequate supply of a component or material, we might have to use a substitute component or material, which could require us to make changes in our manufacturing process. From time to time in the past, we have experienced difficulties in receiving shipments from one or more of our suppliers, especially during periods of high demand for our products. If we cannot obtain an adequate supply of the components and materials we require, or do not receive them in a timely manner, we might be required to identify new suppliers. We might not be able to identify new suppliers on a timely basis or at all. Our customers and we would also need to qualify any new suppliers. The lead-time required to identify and qualify new suppliers could affect our ability to timely ship our products and cause our operating results to suffer. Further, a sole or limited source supplier could require us to enter into non-cancelable purchase commitments or pay in advance to ensure our source of supply. In an industry downturn, commitments of this type could result in charges for excess inventory of parts. If we are unable to predict our component and materials needs accurately, or if our supply is disrupted, we might miss market opportunities by not being able to meet the demand for our products.

Wafer probe cards that do not meet specifications or that contain defects could damage our reputation, decrease market acceptance of our technology, cause us to lose customers and revenues, and result in liability to us.

The complexity and ongoing development of our wafer probe card manufacturing process, combined with increases in wafer probe card production volumes, have in the past and could in the future lead to design or manufacturing problems. For example, the presence of contaminants in our plating baths has caused a decrease in our manufacturing yields or has resulted in unanticipated stress-related failures when our wafer probe cards are being used in the manufacturing test environment. Manufacturing design errors such as the miswiring of a wafer probe card or the incorrect placement of probe contact elements have caused us to repeat manufacturing design steps. In addition to these examples, problems might result from a number of factors, including design defects, materials failures, contamination in the manufacturing environment, impurities in the materials used, unknown sensitivities to process conditions, such as temperature and humidity, and equipment failures. As a result, our products have in the past contained and might in the future contain undetected errors or defects. Any errors or defects could:

cause lower than anticipated yields and lengthening of delivery schedules;

cause delays in product shipments;

cause delays in new product introductions;

cause us to incur warranty expenses;

result in increased costs and diversion of development resources;

cause us to incur increased charges due to unusable inventory;

require design modifications; or

decrease market acceptance or customer satisfaction with these products.

The occurrence of any one or more of these events could hurt our operating results.

In addition, if any of our products fails to meet specifications or has reliability, quality or compatibility problems, our reputation could be damaged significantly and customers might be reluctant to buy our products, which could result in a decline in revenues, an increase in product returns or warranty costs and the loss of existing customers or the failure to attract new customers. Our customers use our products with test equipment and software in their manufacturing facilities. Our products must be compatible with the customers equipment and software to form an integrated system. If the system does not function properly, we could be required to provide field application engineers to locate the problem, which can take time and resources. If the problem relates to our wafer probe cards, we might have to invest significant capital, manufacturing capacity and other resources to correct it. Our current or potential customers also might seek to recover from us any losses resulting

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from defects or failures in our products. Liability claims could require us to spend significant time and money in litigation or to pay significant damages.

If we fail to forecast demand for our products accurately, we could incur inventory losses.

Each semiconductor chip design requires a custom wafer probe card. Because our products are design-specific, demand for our products is difficult to forecast. Due to our customers short delivery time requirements, we often design, and at times produce, our products in anticipation of demand for our products rather than in response to an order. Due to the uncertainty inherent in forecasts, we are and expect to continue to be subject to inventory risk. If we do not obtain orders as we anticipate, we could have excess inventory for a specific customer design that we would not be able to sell to any other customer, which would likely result in inventory write-offs.

If we fail to effectively manage our regional service centers, our business might be harmed.

In 2002, we opened a regional repair and service center in Seoul, South Korea, and in 2003, we opened a regional repair and service center in Dresden, Germany. These regional service centers are part of our strategy to, among other things, provide our customers with more efficient service and repair of our wafer probe cards. If we are unable to effectively manage our regional service centers, or if the work undertaken in the regional service centers is not equivalent to the level and quality provided by repairs and services performed by our North American repair and service operations, which are part of our manufacturing facility in Livermore, California, we could incur higher wafer probe card repair and service costs, which could harm our operating results.

If we do not effectively manage changes in our business, these changes could place a significant strain on our management and operations and, as a result, our business might not succeed.

Our ability to grow successfully requires an effective planning and management process. We plan to increase the scope of our operations and the size of our direct sales force domestically and internationally. For example, we have leased a new facility in Livermore, California and plan to move our corporate headquarters and manufacturing operations into this facility in 2004. Our growth could place a significant strain on our management systems, infrastructure and other resources. To manage our growth effectively, we must invest the necessary capital and continue to improve and expand our systems and infrastructure in a timely and efficient manner. Those resources might not be available when we need them, which would limit our growth. Our officers have limited experience in managing large or rapidly growing businesses. In addition, the majority of our management has no experience in managing a public company or communicating with securities analysts and public company investors. Our controls, systems and procedures might not be adequate to support a growing public company. If our management fails to respond effectively to changes in our business, our business might not succeed.

If we fail to attract and retain qualified personnel, our business might be harmed.

Our future success depends largely upon the continued service of our key management, technical, and sales and marketing personnel, and on our continued ability to hire, integrate and retain qualified individuals, particularly engineers and sales and marketing personnel in order to increase market awareness of our products and to increase revenues. For example, in the future, we might need technical personnel experienced in competencies that we do not currently have or require. Competition for these employees may be intense, and we might not be successful in attracting or retaining these personnel. The loss of any key employee, the failure of any key employee to perform in his or her current position or our inability to attract and retain skilled employees as needed could impair our ability to meet customer and technological demands. All of our key personnel in the United States are employees at-will. We have no employment contracts with any of our personnel in the United States.

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We may make acquisitions, which could put a strain on our resources, cause ownership dilution to our stockholders and adversely affect our financial results.

While we have made no acquisitions of businesses, products or technologies in the past, we may make acquisitions of complementary businesses, products or technologies in the future. Integrating newly acquired businesses, products or technologies into our company could put a strain on our resources, could be expensive and time consuming, and might not be successful. Future acquisitions could divert our management s attention from other business concerns and expose our business to unforeseen liabilities or risks associated with entering new markets. In addition, we might lose key employees while integrating new organizations. Consequently, we might not be successful in integrating any acquired businesses, products or technologies, and might not achieve anticipated revenues and cost benefits. In addition, future acquisitions could result in customer dissatisfaction, performance problems with an acquired company, potentially dilutive issuances of equity securities or the incurrence of debt, contingent liabilities, possible impairment charges related to goodwill or other intangible assets or other unanticipated events or circumstances, any of which could harm our business.

As part of our sales process, we could incur substantial sales and engineering expenses that do not result in revenues, which would harm our operating results.

Our customers generally expend significant efforts evaluating and qualifying our products prior to placing an order. The time that our customers require to evaluate and qualify our wafer probe cards is typically between three and 12 months and sometimes longer. While our customers are evaluating our products, we might incur substantial sales, marketing, and research and development expenses. For example, we typically expend significant resources educating our prospective customers regarding the uses and benefits of our wafer probe cards and developing wafer probe cards customized to the potential customer s needs, for which we might not be reimbursed. Although we commit substantial resources to our sales efforts, we might never receive any revenues from a customer. For example, many semiconductor designs never reach production, including designs for which we have expended design effort and expense. In addition, prospective customers might decide not to use our wafer probe cards. The length of time that it takes for the evaluation process and for us to make a sale depends upon many factors including:

the efforts of our sales force and our distributor and independent sales representatives;

the complexity of the customer s fabrication processes;

the internal technical capabilities of the customer; and

the customer s budgetary constraints and, in particular, the customer s ability to devote resources to the evaluation process.

In addition, product purchases are frequently subject to delays, particularly with respect to large customers for which our products may represent a small percentage of their overall purchases. As a result, our sales cycles are unpredictable. If we incur substantial sales and engineering expenses without generating revenues, our operating results could be harmed.

From time to time, we might be subject to claims of infringement of other parties proprietary rights, or to claims that our intellectual property rights are invalid or unenforceable, which could result in significant expense and loss of intellectual property rights.

In the future, we might receive claims that we are infringing intellectual property rights of others, or claims that our patents or other intellectual property rights are invalid or unenforceable. We have received in the past, and may receive in the future, communications from third parties inquiring about our interest in licensing certain of their intellectual property or more generally identifying intellectual property that may be of interest to us. For example, we received such a communication from Microelectronics and Computer Technology Corporation in October 2001, with a follow-up letter in January 2002, inquiring about our interest in acquiring a license to certain of their patents and technology, and from IBM Corporation in February 2002, with a follow-up letter in August 2003, inquiring about our interest and need to acquire a license to IBM patents and technology related to high density integrated probes. We have not engaged in a dialog with Microelectronics and Computer Technology

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Corporation; we presently anticipate that we will engage in a dialog with IBM Corporation regarding our companies respective intellectual property portfolios. In August 2002, subsequent to our initiating correspondence with Japan Electronic Materials Corporation regarding the scope of our intellectual property rights and the potential applicability of those rights to certain of its wafer probe cards, Japan Electronic Materials Corporation offered that precedent technologies exist as to one of our foreign patents that we had identified, and also referenced a U.S. patent in which it stated we might take interest. For the inquiries we have received to date, we do not believe we infringe any of the identified patents and technology. The semiconductor industry is characterized by uncertain and conflicting intellectual property claims and vigorous protection and pursuit of these rights. The resolution of any claims of this nature, with or without merit, could be time consuming, result in costly litigation or cause product shipment delays. In the event of an adverse ruling, we might be required to pay substantial damages, cease the use or sale of infringing products, spend significant resources to develop non-infringing technology, discontinue the use of certain technology or enter into license agreements. License agreements, if required, might not be available on terms acceptable to us or at all. The loss of access to any of our intellectual property or the ability to use any of our technology could harm our business.

If we fail to protect our proprietary rights, our competitors might gain access to our technology, which could adversely affect our ability to compete successfully in our markets and harm our operating results.

If we fail to protect our proprietary rights adequately, our competitors might gain access to our technology. Unauthorized parties might attempt to copy aspects of our products or to obtain and use information that we regard as proprietary. Others might independently develop similar or competing technologies or methods or design around our patents. In addition, the laws of many foreign countries in which we or our customers do business do not protect our intellectual property rights to the same extent as the laws of the United States. As a result, our competitors might offer similar products and we might not be able to compete successfully. We also cannot assure that:

- our means of protecting our proprietary rights will be adequate;
- patents will be issued from our currently pending or future applications;
- our existing patents or any new patents will be sufficient in scope or strength to provide any meaningful protection or commercial advantage to us;
- any patent, trademark or other intellectual property right that we own will not be invalidated, circumvented or challenged in the United States or foreign countries; or
- others will not misappropriate our proprietary technologies or independently develop similar technology, duplicate our products or design around any patent or other intellectual property rights that we own.

We might be required to spend significant resources to monitor and protect our intellectual property rights. We presently believe that it is likely that one or more of our competitors are using methodologies or have implemented structures into certain of their products that are covered by one or more of our intellectual property rights. We may initiate claims or litigation against third parties for infringement of our proprietary rights or to establish the validity of our proprietary rights. If we threaten or initiate litigation, we may be subject to claims by third parties against which we must defend. Any litigation, whether or not it is resolved in our favor, could result in significant expense to us and divert the efforts of our technical and management personnel. In addition, many of our customer contracts contain provisions that require us to indemnify our customers for third party intellectual property infringement claims, which would increase the cost to us of an adverse ruling in such a claim. An adverse determination could also prevent us from licensing our technologies and methods to others.

Our failure to comply with environmental laws and regulations could subject us to significant fines and liabilities, and new laws and regulations or changes in regulatory interpretation or enforcement could make compliance more difficult and costly.

We are subject to various and frequently changing U.S. federal, state and local, and foreign governmental laws and regulations relating to the protection of the environment, including those governing the discharge of

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pollutants into the air and water, the management and disposal of hazardous substances and wastes, the cleanup of contaminated sites and the maintenance of a safe workplace. We could incur substantial costs, including cleanup costs, civil or criminal fines or sanctions and third-party claims for property damage or personal injury, as a result of violations of or liabilities under environmental laws and regulations or non-compliance with the environmental permits required at our facilities. For instance, in May 2003, we received a Notice of Violation from the Bay Area Air Quality Management District regarding our record keeping relating to our usage of wipe cleaning solvent. We introduced corrective action to prevent any continued or recurrent record keeping violation, and we resolved the Notice of Violation with a monetary payment which was not significant. It is possible that in the future, we may receive environmental violation notices, and that final resolution of the violations identified by these notices could harm our operating results.

These laws, regulations and permits also could require the installation of costly pollution control equipment or operational changes to limit pollution emissions or decrease the likelihood of accidental releases of hazardous substances. In addition, new laws and regulations, stricter enforcement of existing laws and regulations, the discovery of previously unknown contamination at our or others sites or the imposition of new cleanup requirements could require us to curtail our operations, restrict our future expansion, subject us to liability and cause us to incur future costs that would have a negative effect on our operating results and cash flow.

Because we conduct some of our business internationally, we are subject to operational, economic, financial and political risks abroad.

Sales of our products to customers outside the United States have accounted for an important part of our revenues. Our international sales as a percentage of our revenues were 43.5% for the nine months ended September 27, 2003 and 44.4% for fiscal 2002. In the future, we expect international sales, particularly into Europe, Japan, South Korea and Taiwan, to continue to account for a significant percentage of our revenues. Accordingly, we will be subject to risks and challenges that we would not otherwise face if we conducted our business only in the United States. These risks and challenges include:

- compliance with a wide variety of foreign laws and regulations;
- legal uncertainties regarding taxes, tariffs, quotas, export controls, export licenses and other trade barriers;
- political and economic instability in, or foreign conflicts that involve or affect, the countries of our customers;
- difficulties in collecting accounts receivable and longer accounts receivable payment cycles;
- difficulties in staffing and managing personnel, distributors and representatives;
- reduced protection for intellectual property rights in some countries;
- currency exchange rate fluctuations, which could affect the value of our assets denominated in local currency, as well as the price of our products relative to locally produced products;
- seasonal fluctuations in purchasing patterns in other countries; and
- fluctuations in freight rates and transportation disruptions.

Any of these factors could harm our existing international operations and business or impair our ability to continue expanding into international markets.

An outbreak of SARS and its spread could harm sales of our products.

If an outbreak of severe acute respiratory syndrome, or SARS, that began in China, Hong Kong, Singapore and Vietnam recurs, it may have a negative impact on our business. Our business may be impacted by a number of SARS-related factors, including, but not limited to, disruptions in the operations of our customers and their partners, reduced sales in certain end-markets, such as DRAM devices, and increased costs to conduct our business abroad. If the number of cases of SARS rises or spreads, our sales could potentially be harmed.

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We might require additional capital to support business growth, and such capital might not be available.

We intend to continue to make investments to support business growth and may require additional funds to respond to business challenges, which include the need to develop new products or enhance existing products, enhance our operating infrastructure and acquire complementary businesses and technologies. Accordingly, we may need to engage in equity or debt financing to secure additional funds. Equity and debt financing, however, might not be available when needed or, if available, might not be available on terms satisfactory to us. If we are unable to obtain adequate financing or financing on terms satisfactory to us, our ability to continue to support our business growth and to respond to business challenges could be significantly limited.

Our reported financial results may be adversely affected by changes in accounting principles generally accepted in the United States.

We prepare our financial statements in conformity with accounting principles generally accepted in the United States. These accounting principles are subject to interpretation by the Financial Accounting Standards Board, the American Institute of Certified Public Accountants, the Securities and Exchange Commission and various bodies formed to interpret and create appropriate accounting principles. A change in these principles or interpretations could have a significant effect on our reported financial results, and could affect the reporting of transactions completed before the announcement of a change.

Recently enacted and proposed changes in securities laws and regulations are likely to increase our costs.

The Sarbanes-Oxley Act of 2002 that became law in July 2002, as well as new rules subsequently implemented by the Securities and Exchange Commission, have required changes to some of our corporate governance practices. The Act also requires the Securities and Exchange Commission to promulgate additional new rules on a variety of subjects. In addition to final rules and rule proposals already made by the Securities and Exchange Commission, Nasdaq has proposed revisions to its requirements for companies, such as us, that are Nasdaq-listed. We expect these new rules and regulations to increase our legal and financial compliance costs, and to make some activities more difficult, time consuming and/or costly. We also expect these new rules and regulations to make it more difficult and more expensive for us to obtain director and officer liability insurance, and we may be required to accept reduced coverage or incur substantially higher costs to obtain coverage. These new rules and regulations could also make it more difficult for us to attract and retain qualified members of our board of directors, particularly to serve on our audit committee, and qualified executive officers.

Risks Related to this Offering

The trading price of our common stock is likely to be volatile, and you might not be able to sell your shares at or above the public offering price for this offering.

The trading prices of the securities of technology companies have been highly volatile. Accordingly, the trading price of our common stock is likely to be subject to wide fluctuations. Further, our securities have a limited trading history. Factors affecting the trading price of our common stock include:

- variations in our operating results;
- announcements of technological innovations, new products or product enhancements, strategic alliances or significant agreements by us or by our competitors;
- recruitment or departure of key personnel;
- the gain or loss of significant orders or customers;
- changes in the estimates of our operating results or changes in recommendations by any securities analysts that elect to follow our common stock; and
- market conditions in our industry, the industries of our customers and the economy as a whole.

In addition, if the market for technology stocks or the stock market in general experiences continued or greater loss of investor confidence, the trading price of our common stock could decline for reasons unrelated to

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our business, operating results or financial condition. The trading price of our common stock also might decline in reaction to events that affect other companies in our industry even if these events do not directly affect us.

If securities analysts do not publish research or reports about our business, our stock price could decline.

The trading market for our common stock will rely in part on the research and reports that industry or financial analysts publish about us or our business. We do not control these analysts. If one or more of the analysts who cover us downgrade our stock, our stock price would likely decline rapidly. If one or more of these analysts cease coverage of our company, we could lose visibility in the market, which in turn could cause our stock price to decline.

The concentration of our capital stock ownership with insiders upon the completion of this offering will likely limit your ability to influence corporate matters.

We anticipate that our executive officers, directors, current 5% or greater stockholders and entities affiliated with any of them will together beneficially own approximately 44.6% of our common stock outstanding after this offering. As a result, these stockholders, acting together, will have substantial influence over all matters that require approval by our stockholders, including the election of directors and approval of significant corporate transactions. As a result, corporate actions might be taken even if other stockholders, including those who purchase shares in this offering, oppose them. This concentration of ownership might also have the effect of delaying or preventing a change of control of our company that other stockholders may view as beneficial.

Our management will have broad discretion over the use of the proceeds to us from this offering and might not apply the proceeds of this offering in ways that increase the value of your investment.

Our management will have broad discretion to use the net proceeds to us from this offering, and you will be relying on the judgment of our management regarding the application of these proceeds. We intend to use a portion of the net proceeds to us from this offering for leasehold improvements at our new corporate headquarters and manufacturing facility. Although we expect our management to use the remaining net proceeds from this offering for general corporate purposes, including working capital and for potential strategic investments or acquisitions, we have not allocated these net proceeds for specific purposes. Our management might not be able to yield a significant return, if any, on any investment of these net proceeds.

Future sales of shares by existing stockholders could cause our stock price to decline.

If our existing stockholders sell, or indicate an intention to sell, substantial amounts of our common stock in the public market after the contractual lock-ups and other legal restrictions on resale discussed in this prospectus lapse, the trading price of our common stock could decline below the public offering price for this offering. Based on the shares outstanding as of September 27, 2003, and assuming 5,000,000 shares are sold in this offering, upon completion of this offering we will have outstanding approximately 35,791,828 shares of common stock. Of these shares, 11,900,000 shares are freely tradeable, without restriction, in the public market, except for any shares that are held by our affiliates. An additional 436,000 shares of our common stock are eligible for sale in the public market; however, if any of these shares are not sold by November 15, 2003, they will be subject to contractual lock-up restrictions with us and lock-up agreements with Morgan Stanley & Co. Incorporated which expire at the close of business on December 8, 2003, after which time such unsold shares will be eligible for sale in the public market. Morgan Stanley & Co. Incorporated has also released 766,165 shares of our common stock from lock-up agreements; however, these shares remain subject to the contractual lock-up restrictions with us, and will not be eligible for sale in the public market until after December 8, 2003. An additional 12,129,134 shares of our common stock will also become eligible for sale in the public market after December 8, 2003 when the contractual lock-up restrictions with us and lock-up agreements with Morgan Stanley & Co. Incorporated expire. Of the remaining 11,316,616 shares of our common stock subject to lock-up agreements with Morgan Stanley & Co. Incorporated, 5,658,308 shares will become eligible for sale in the public market on February 15, 2004, and 5,658,308 shares will become eligible for sale in the public market on March 15, 2004. Upon the expiration of, or release from, the lock-up restrictions, the shares will be eligible for sale in the

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public market only to the extent permitted by the provisions of various vesting agreements, and Rules 144 and 701 under the Securities Act.

In addition, the 118,227 shares subject to outstanding warrants and the 10,760,992 shares subject to outstanding options and reserved for future issuance under our stock option and purchase plans will become eligible for sale in the public market to the extent permitted by the provisions of various vesting agreements, the lock-up agreements and Rules 144 and 701 under the Securities Act. If these additional shares are sold, or if it is perceived that they will be sold, in the public market, the trading price of our common stock could decline. See Shares Eligible for Future Sale for more information regarding shares of our common stock that existing stockholders may sell after this offering.

You will experience immediate and substantial dilution in the net tangible book value of the shares you purchase in this offering.

The public offering price of our common stock in this offering is substantially higher than the book value per share of the outstanding common stock after this offering. Therefore, based on an assumed public offering price of $25.47 per share, if you purchase our common stock in this offering, you will suffer immediate and substantial dilution of approximately $20.24 per share. If the underwriters exercise their over-allotment option, or if outstanding options and warrants to purchase our common stock are exercised, you will experience additional dilution.

Provisions of our certificate of incorporation and bylaws or Delaware law might discourage, delay or prevent a change of control of our company or changes in our management and, therefore, depress the trading price of our common stock.

Delaware corporate law and our certificate of incorporation and bylaws contain provisions that could discourage, delay or prevent a change in control of our company or changes in our management that the stockholders of our company may deem advantageous. These provisions:

- establish a classified board of directors so that not all members of our board are elected at one time;
- provide that directors may only be removed for cause and only with the approval of 66 2/3% of our stockholders;
- require super-majority voting to amend some provisions in our certificate of incorporation and bylaws;
- authorize the issuance of blank check preferred stock that our board could issue to increase the number of outstanding shares and to discourage a takeover attempt;
- limit the ability of our stockholders to call special meetings of stockholders;
- prohibit stockholder action by written consent, which requires all stockholder actions to be taken at a meeting of our stockholders;
- provide that the board of directors is expressly authorized to make, alter or repeal our bylaws; and
- establish advance notice requirements for nominations for election to our board or for proposing matters that can be acted upon by stockholders at stockholder meetings.

In addition, Section 203 of the Delaware General Corporation Law may discourage, delay or prevent a change in control of our company.

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SPECIAL NOTE REGARDING FORWARD-LOOKING STATEMENTS

We have made statements under the captions Prospectus Summary, Risk Factors, Management s Discussion and Analysis of Financial Condition and Results of Operations and Business and in other sections of this prospectus that are forward-looking statements. In some cases, you can identify these statements by forward-looking words such as may, might, will, could, should, expect, plan, anticipate, belie predict, potential or continue, the negative or plural of these words and other comparable terminology. These forward-looking statements, which are subject to risks, uncertainties and assumptions about us, include statements concerning, among other things, our business strategy, anticipated trends or developments in our business and the markets in which we operate, revenues, gross margin, operating expenses, research and development programs, sales and marketing initiatives, and competition. These statements are only predictions based on our current expectations and projections about future events. You should not place undue reliance on these forward-looking statements. We undertake no obligation to update any of these statements for any reason. These forward-looking statements involve known and unknown risks, uncertainties and other factors that may cause our actual results, levels of activity, performance or achievements to differ materially from those expressed or implied by these statements. These factors include the matters discussed under the caption entitled Risk Factors. You should carefully consider the numerous risks and uncertainties described under Risk Factors.

You should read this prospectus and the documents that we reference in this prospectus and have filed as exhibits to the registration statement on Form S-1, of which this prospectus is a part, that we have filed with the Securities and Exchange Commission, completely and with the understanding that our actual future results, levels of activity, performance and achievements may be materially different from what we expect. We qualify all of our forward-looking statements by these cautionary statements.

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USE OF PROCEEDS

We estimate that the net proceeds we will receive from this offering will be approximately $36.5 million, at an assumed public offering price of $25.47 per share, after deducting estimated underwriting discounts and commissions and estimated offering costs. If the underwriters exercise their over-allotment option in full, we estimate that our net proceeds will be approximately $54.7 million. The selling stockholders will receive aggregate net proceeds of approximately $85.1 million, after deducting estimated underwriting discounts and commissions. We will not receive any proceeds from the sale of shares of common stock by the selling stockholders.

We intend to use the net proceeds to us from this offering for general corporate purposes and working capital requirements. We may also use a portion of the net proceeds to us to fund possible investments in, or acquisitions of, complementary businesses, products or technologies or establishing joint ventures. We have no current agreements or commitments with respect to any investment, acquisition or joint venture, and we currently are not engaged in negotiations with respect to any investment, acquisition or joint venture. Pending their ultimate use, we intend to invest the net proceeds to us from this offering in short-term, interest-bearing, investment grade securities.

The amount and timing of what we actually spend for these purposes may vary significantly and will depend on a number of factors, including our future revenues and cash generated by operations and the other factors described in Risk Factors. Therefore, we will have broad discretion in the way we use the net proceeds to us from this offering.

PRICE RANGE OF COMMON STOCK

Our common stock has been quoted on the Nasdaq National Market under the symbol FORM since June 12, 2003. Prior to this time, there was no public market for our common stock. The following table sets forth, for the periods indicated in fiscal 2003, the high and low sale prices per share for our common stock as reported on the Nasdaq National Market.

	Common Stock Price	
	High	**Low**
Second Quarter (from June 12, 2003)	$21.00	$16.21
Third Quarter	23.07	17.00
Fourth Quarter (through October 17, 2003)	27.45	20.00

On October 17, 2003, the last reported sales price for our common stock on the Nasdaq National Market was $25.47 per share. As of September 27, 2003, there were approximately 312 holders of record of our common stock.

DIVIDEND POLICY

We have never declared or paid cash dividends on our capital stock. We currently expect to retain all available funds and any future earnings for use in the operation and development of our business. Accordingly, we do not anticipate declaring or paying cash dividends on our common stock in the foreseeable future. In addition, the terms of our loan and security agreement prohibit us from paying cash dividends without the prior consent of the bank.

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CAPITALIZATION

The following table sets forth our capitalization as of September 27, 2003. Our capitalization is presented on an actual basis and on an as adjusted basis to reflect the sale of 1,499,866 shares of our common stock offered by us at an assumed public offering price of $25.47 per share, after deducting estimated underwriting discounts and commissions and estimated offering costs payable by us, and the proceeds from the exercise of options to purchase 27,629 shares of common stock by four selling stockholders in this offering. This capitalization table should be read together with Selected Consolidated Financial Data and Management s Discussion and Analysis of Financial Condition and Results of Operations and our consolidated financial statements and related notes included elsewhere in this prospectus.

	September 27, 2003	
	Actual	As Adjusted
	(in thousands, except share and per share data)	
Stockholders equity:		
Preferred stock, $.001 par value; 10,000,000 shares authorized, no shares issued or outstanding, actual; 10,000,000 shares authorized, no shares issued or outstanding, as adjusted	$	$
Common stock, $.001 par value; 250,000,000 shares authorized, 34,264,333 shares issued and outstanding, actual; 250,000,000 shares authorized, 35,791,828 shares issued and outstanding, as adjusted	34	35
Additional paid-in capital	168,698	205,337
Notes receivable from stockholders	(1,389)	(1,389)
Deferred stock-based compensation, net	(12,007)	(12,007)
Accumulated other comprehensive loss	(18)	(18)
Accumulated deficit	(4,874)	(4,874)
Total stockholders equity	150,444	187,084
Total capitalization	$150,444	$187,084

The number of shares of our common stock shown as issued and outstanding in the table above excludes:

7,050,111 shares of common stock issuable upon exercise of options outstanding at September 27, 2003 with a weighted average exercise price of $8.25 per share, which amount includes 27,629 shares of common stock subject to options that will be exercised by four selling stockholders in this offering. We have included the 27,629 shares in our calculation of our shares outstanding after this offering;

118,227 shares of common stock issuable upon exercise of warrants outstanding at September 27, 2003 with a weighted average exercise price of $5.25 per share;

2,210,881 shares of common stock available for issuance under our equity incentive plan at September 27, 2003; and

1,500,000 shares of common stock available for issuance under our employee stock purchase plan at September 27, 2003.

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DILUTION

Our net tangible book value as of September 27, 2003 was approximately $150.4 million, or $4.39 per share of our common stock. Our net tangible book value per share represents our total tangible assets less total liabilities divided by the number of shares of our common stock outstanding on September 27, 2003.

After giving effect to the sale of 1,499,866 shares of common stock offered by us in this offering at an assumed public offering price of $25.47 per share, after deducting estimated underwriting discounts and commissions and estimated offering costs payable by us, and the proceeds from the exercise of options to purchase 27,629 shares of common stock by four selling stockholders in this offering, our net tangible book value as of September 27, 2003 would have been approximately $187.1 million, or $5.23 per share of our common stock. This amount represents an immediate increase in net tangible book value of $0.84 per share to our existing stockholders and an immediate dilution in net tangible book value of $20.24 per share to new investors purchasing shares in this offering. The following table illustrates the dilution in net tangible book value per share to new investors.

Assumed public offering price per share		$25.47
Net tangible book value per share as of September 27, 2003	$4.39	
Increase per share attributable to new investors	.84	
Net tangible book value per share after this offering		5.23
Dilution in net tangible book value per share to new investors		$20.24

If all of our then outstanding options and warrants were exercised, the net tangible book value as of September 27, 2003 would have been $245.9 million and the net tangible book value after this offering would have been $5.72 per share, causing dilution to new investors of $0.50 per share.

The following table summarizes, as of September 27, 2003 on the basis described above, the number of shares of our common stock purchased from us, the total consideration paid to us, and the average price per share paid to us by existing stockholders and to be paid by new investors purchasing shares of our common stock in this offering at an assumed public offering price of $25.47 per share, before deducting estimated underwriting discounts and commissions and estimated offering costs payable by us.

	Shares Purchased		Total Consideration		Average Price Per Share
	Number	Percent	Amount	Percent	
Existing stockholders	34,264,333	95.7%	$153,801,000	80.0%	$ 4.49
New investors	1,527,495	4.3	38,359,476	20.0	25.11
Total	35,791,828	100.0%	$192,160,476	100.0%	

The above information excludes:

7,050,111 shares of common stock issuable upon exercise of options outstanding at September 27, 2003 with a weighted average exercise price of $8.25 per share, which amount includes 27,629 shares of common stock subject to options that will be exercised by four selling stockholders in this offering. For purposes of calculating dilution, however, we have considered the 27,629 shares to be outstanding after this offering;

118,227 shares of common stock issuable upon exercise of warrants outstanding at September 27, 2003 with a weighted average exercise price of $5.25 per share;

2,210,881 shares of common stock available for issuance under our equity incentive plan at September 27, 2003; and

1,500,000 shares of common stock available for issuance under our employee stock purchase plan at September 27, 2003.

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SELECTED CONSOLIDATED FINANCIAL DATA

The selected consolidated financial data should be read in conjunction with Management s Discussion and Analysis of Financial Condition and Results of Operations and our consolidated financial statements and the related notes appearing elsewhere in this prospectus. The consolidated statement of operations data for the fiscal years ended December 30, 2000, December 29, 2001 and December 28, 2002, and the consolidated balance sheet data as of December 29, 2001 and December 28, 2002, are derived from our audited consolidated financial statements appearing elsewhere in this prospectus. The consolidated statement of operations data for the fiscal years ended December 26, 1998 and December 25, 1999 and the consolidated balance sheet data as of December 26, 1998, December 25, 1999 and December 30, 2000, are derived from our audited consolidated financial statements that are not included in this prospectus. The consolidated statement of operations data for the nine months ended September 28, 2002 and September 27, 2003, and the consolidated balance sheet data as of September 27, 2003, are derived from our unaudited consolidated financial statements appearing elsewhere in this prospectus. We have prepared the unaudited information on the same basis as the audited consolidated financial statements and have included, in our opinion, all adjustments, consisting only of normal and recurring adjustments, that we consider necessary for a fair presentation of the financial information set forth in those statements. The historical results are not necessarily indicative of the results to be expected in any future period.

	Fiscal Year Ended					Nine Months Ended	
	Dec. 26, 1998	Dec. 25, 1999	Dec. 30, 2000	Dec. 29, 2001	Dec. 28, 2002	Sept. 28, 2002	Sept. 27, 2003
	(in thousands, except per share data)						
Consolidated Statement of Operations Data:							
Revenues	$19,329	$35,722	$56,406	$73,433	$78,684	$56,527	$66,839
Cost of revenues	10,763	20,420	28,243	38,385	39,456	28,540	34,482
Gross margin	8,566	15,302	28,163	35,048	39,228	27,987	32,357
Operating expenses:							
Research and development	7,486	9,466	11,995	14,619	14,592	10,656	11,322
Selling, general and administrative	7,212	11,020	15,434	18,500	17,005	12,429	13,471
Stock-based compensation		341	259	469	1,039	750	1,100
Restructuring charges				1,380			
Total operating expenses	14,698	20,827	27,688	34,968	32,636	23,835	25,893
Operating income (loss)	(6,132)	(5,525)	475	80	6,592	4,152	6,464
Interest and other income (expense), net	157	(119)	1,719	477	642	404	780
Income (loss) before income taxes	(5,975)	(5,644)	2,194	557	7,234	4,556	7,244
Benefit (provision) for income taxes			(115)	(307)	3,125	4,214	(2,753)
Net income (loss)	$ (5,975)	$ (5,644)	$ 2,079	$ 250	$10,359	$ 8,770	$ 4,491
Net income (loss) per share:							
Basic	$ (3.60)	$ (2.16)	$ .61	$ .06	$ 2.33	$ 1.98	$ .27
Diluted	$ (3.60)	$ (2.16)	$ .08	$ .01	$ .35	$ .30	$ .14
Weighted-average number of shares used in per share calculations:							
Basic	1,659	2,609	3,408	4,029	4,448	4,436	16,669
Diluted	1,659	2,609	26,821	28,654	29,554	29,287	32,932

	As of					
	Dec. 26, 1998	Dec. 25, 1999	Dec. 30, 2000	Dec. 29, 2001	Dec. 28, 2002	Sept. 27, 2003

						(unaudited)
			(in thousands)			
Consolidated Balance Sheet Data:						
Cash, cash equivalents and short-term investments	$ 10,449	$ 19,248	$ 16,897	$ 27,576	$ 34,343	$ 101,084
Working capital	8,032	17,694	23,391	31,074	40,536	110,465
Total assets	22,532	38,332	47,499	62,264	77,518	170,254
Long-term debt, less current portion	2,834	2,183	521	1,167	625	
Redeemable convertible preferred stock and warrants	27,963	47,913	55,129	65,201	65,201	
Deferred stock-based compensation, net		(184)	(184)	(4,071)	(12,294)	(12,007)
Total stockholders equity (deficit)	(15,889)	(21,286)	(18,586)	(17,582)	(5,037)	150,444

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MANAGEMENT S DISCUSSION AND ANALYSIS OF

FINANCIAL CONDITION AND RESULTS OF OPERATIONS

The following discussion and analysis of our financial condition and results of operations should be read in conjunction with Selected Consolidated Financial Data and our consolidated financial statements and the related notes included elsewhere in this prospectus. In addition to historical consolidated financial information, the following discussion and analysis contains forward-looking statements that involve risks, uncertainties and assumptions. Our actual results could differ materially from those anticipated by these forward-looking statements as a result of many factors, including those discussed under Risk Factors and elsewhere in this prospectus.

Overview

We design, develop, manufacture, sell and support precision, high performance advanced semiconductor wafer probe cards. At the core of our product offering is our proprietary MicroSpring interconnect technology. Our MicroSpring interconnect technology includes a resilient contact element manufactured at our production facilities in Livermore, California. To date, we have derived our revenues primarily from the sale of wafer probe cards incorporating our MicroSpring interconnect technology.

We were formed in 1993 and in 1995 introduced our first commercial product. During 1996, we introduced the industry s first memory wafer probe card capable of testing up to 32 devices in parallel. Our revenues increased from $1.1 million in fiscal 1995 to $78.7 million in fiscal 2002.

We work closely with our customers to design, develop and manufacture custom wafer probe cards. Each wafer probe card is a custom product that is specific to the chip and wafer designs of the customer. As a result, our revenue growth is driven by the number of new semiconductor designs, technology transitions and increased semiconductor production volumes.

While the majority of our sales are directly to semiconductor manufacturers, we also have significant sales to our distributor in Taiwan. Sales to our distributors were 15.1% of revenues in the nine months ended September 27, 2003, 22.6% of revenues in fiscal 2002, 32.9% of revenues in fiscal 2001 and 40.6% of revenues in fiscal 2000. We sold our products in Japan to a distributor until March 31, 2002, when we began to sell directly in Japan. Currently, we have one distributor, Spirox Corporation, which serves Taiwan, Singapore and China. We also have the ability to sell our products directly to customers in that region.

Because our products serve the highly cyclical semiconductor industry, our business is subject to demand fluctuations that have resulted in significant variations of revenues, expenses and results of operations in the periods presented. Fluctuations are likely to continue in future periods. Due to a high concentration of large customers in the semiconductor industry, we believe that sales to a limited number of customers will continue to account for a substantial part of our business. We generally have limited backlog and therefore we rely upon orders that are booked and shipped in the same quarter for a majority of our revenues.

Fiscal Year. Our fiscal year ends on the last Saturday in December. The fiscal year ended December 28, 2002 had 52 weeks, the fiscal year ended December 29, 2001 had 52 weeks, and the fiscal year ended December 30, 2000 had 53 weeks.

Revenues. We derive our revenues from product sales, license and development fees and royalties. To date, wafer probe card sales have comprised substantially all of our revenues. Wafer probe card sales accounted for 99.8% of our revenues in the nine months ended September 27, 2003, 99.9% of our revenues in fiscal 2002, 99.2% of our revenues in fiscal 2001 and 97.8% of our revenues in fiscal 2000. Revenues from license and development fees and royalties have historically not been significant. Increases in revenues have resulted from increased demand for our existing products, the introduction of new, more complex products and the penetration of new markets. Revenues from our customers are subject to both quarterly and annual fluctuations due to design cycles, technology adoption rates and cyclicality of the different end markets into which our customers products are sold. We expect that revenues from the sale of wafer probe cards will continue to account for substantially all of our revenues for the foreseeable future.

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Cost of Revenues. Cost of revenues consists primarily of manufacturing materials, payroll and manufacturing-related overhead. Our manufacturing operations rely upon a limited number of suppliers to provide key components and materials for our products, some of which are sole source. We order materials and supplies based on backlog and forecasted customer orders. Tooling and setup costs related to changing manufacturing lots at our suppliers are also included in the cost of revenues. We expense all warranty costs and inventory reserves or write-offs as cost of revenues.

We design, manufacture and sell a fully custom product into a market that has been subject to cyclicality and significant demand fluctuations. Wafer probe cards are complex products, custom to a specific chip design and have to be delivered on lead-times shorter than most manufacturers cycle times. It is therefore common to start production and to acquire production materials ahead of the receipt of an actual purchase order. Wafer probe cards are manufactured in low volumes, therefore, material purchases are often subject to minimum purchase order quantities in excess of our actual demand. Inventory valuation adjustments for these factors are considered a normal component of cost of revenues.

Research and Development. Research and development expenses include expenses related to product development, engineering and material costs. All research and development costs are expensed as incurred. We plan to invest a significant amount in research and development activities to develop new technologies for current and new markets and new applications in the future. We expect research and development expenses to increase in absolute dollars, but to decline as a percentage of revenues.

Selling, General and Administrative. Selling, general and administrative expenses include expenses related to sales, marketing and administrative personnel, internal and outside sales representatives commissions, market research and consulting, and other marketing and sales activities. We expect that selling expenses will increase as revenues increase, and we expect that general and administrative expenses will increase in absolute dollars to support future operations, as well as from the additional costs of being a publicly traded company. We expect selling, general and administrative expenses to decline as a percentage of revenues.

Stock-Based Compensation. In connection with the grant of stock options to employees in fiscal 2001 and fiscal 2002, and in fiscal 2003 through our initial public offering in June 2003, we recorded an aggregate of $14.3 million in deferred stock-based compensation. These options are considered compensatory because the fair value of our stock determined for financial reporting purposes is greater than the fair value determined on the date of the grant. As of September 27, 2003, we had an aggregate of $12.0 million of deferred stock-based compensation remaining to be amortized. This deferred stock-based compensation balance will be amortized as follows: $395,000 during the remainder of fiscal 2003; $2.5 million during fiscal 2004; $4.2 million during fiscal 2005; $3.8 million during fiscal 2006 and $1.1 million during fiscal 2007. We are amortizing the deferred stock-based compensation on a straight line basis over the vesting period of the related options, which is generally four years. For options granted to employees to date, the amount of stock-based compensation amortization to be recognized in future periods could decrease if options for which deferred but unvested compensation has been recorded are forfeited.

Provision for Income Taxes. As of December 28, 2002, we had state net operating loss carryforwards of approximately $825,000. The state net operating loss carryforwards will expire at various dates from 2006 through 2013. We also had research and development tax credit carryforwards of approximately $742,000 and $836,000 for federal and state income tax purposes, respectively. The federal research and development tax credit carryforward will expire at various dates from 2019 through 2022. The state research credit can be carried forward indefinitely. In the third quarter of fiscal 2002, we released our valuation allowance recorded against our deferred tax assets because we believe that it is more likely than not that our deferred tax assets will be realized.

Under the Internal Revenue Code, as amended, and similar state provisions, certain substantial changes in our ownership could result in an annual limitation on the amount of net operating loss and credit carryforwards that can be utilized in future years to offset future taxable income. Annual limitations may result in the expiration of net operating loss and credit carryforwards before they are used.

Use of Estimates. Our discussion and analysis of our financial condition and results of operations are based upon our consolidated financial statements, which have been prepared in accordance with accounting principles

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generally accepted in the United States of America. The preparation of these financial statements requires us to make estimates and judgments that affect the reported amount of assets, liabilities, revenues and expenses, and related disclosure of contingent assets and liabilities. On an on-going basis, we evaluate our estimates, including those related to uncollectible receivables, inventories, investments, intangible assets, income taxes, financing operations, warranty obligations, excess component and order cancellation costs, restructuring, and contingencies and litigation. We base our estimates on historical experience and on various other assumptions that are believed to be reasonable under the circumstances, the results of which form the basis for making judgments about the carrying values of assets and liabilities that are not readily apparent from other sources. For excess component costs, the estimates are dependent on our expected use of such components and the size of the minimum order quantity imposed by the vendor in relation to our inventory requirements. Because this can vary in each situation, actual results may differ from these estimates under different assumptions or conditions.

Results of Operations

The following table presents our historical operating results for the periods indicated as a percentage of revenues:

	Fiscal Year Ended			Nine Months Ended	
	Dec. 30, 2000	Dec. 29, 2001	Dec. 28, 2002	Sept. 28, 2002	Sept. 27, 2003
Revenues	100.0%	100.0%	100.0%	100.0%	100.0%
Cost of revenues	50.1	52.3	50.1	50.5	51.6
Gross margin	49.9	47.7	49.9	49.5	48.4
Operating expenses:					
Research and development	21.3	19.9	18.6	18.9	16.9
Selling, general and administrative	27.4	25.2	21.6	22.0	20.2
Stock-based compensation	0.4	0.6	1.3	1.3	1.6
Restructuring charges		1.9			
Total operating expenses	49.1	47.6	41.5	42.2	38.7
Operating income	0.8	0.1	8.4	7.3	9.7
Interest and other income, net	3.1	0.6	0.8	0.7	1.1
Income before income taxes	3.9	0.7	9.2	8.0	10.8
Benefit (provision) for income taxes	(0.2)	(0.4)	4.0	7.5	(4.1)
Net income	3.7%	0.3%	13.2%	15.5%	6.7%

Nine Months Ended September 27, 2003 and September 28, 2002

Revenues. Revenues for the nine months ended September 27, 2003 were $66.8 million compared with $56.5 million for the nine months ended September 28, 2002, an increase of $10.3 million, or 18.2%. The $10.3 million increase for the first nine months of 2003 was due primarily to an increase of $8.1 million in revenues from manufacturers of flash memory devices and an increase of $2.7 million in revenues from manufacturers of microprocessors and chipsets partially offset by a reduction of $418,000 in revenues from sales to other logic manufacturers.

The majority of revenues for the nine months ended September 27, 2003 was generated by sales of wafer probe cards to manufacturers of DRAM devices. Sales of wafer probe cards to test DRAM devices for the nine months ended September 27, 2003 accounted for $38.8 million, or 58.0% of revenues, compared to $38.9 million, or 68.8% of revenues, for the nine months ended September 28, 2002. An increase in revenues from DDR DRAM device manufacturers was offset by a decreased demand for SDRAM products. Sales of wafer probe cards to test DRAM devices benefited from the continued transition of DRAM manufacturers to 512 megabit devices, to 110 nanometer technology and to 300mm wafer size.

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Revenues generated from sales to flash memory device manufacturers for the nine months ended September 27, 2003 were $14.1 million compared with $6.0 million for the nine months ended September 28, 2002. Revenues from flash memory devices increased for the nine months ended September 27, 2003 compared to the nine months ended September 28, 2002 due primarily to increased design and customer wins at manufacturers of flash memory devices.

Revenues from manufacturers of microprocessors and other flip chip devices increased to $13.5 million for the nine months ended September 27, 2003 compared with $10.8 million for the nine months ended September 28, 2002. Revenues for the nine months ended September 27, 2003 benefited from new product introductions, such as our 175 micron pitch MicroSpring contact technology and MicroForce probing technology solutions for flip chip logic applications. These products were introduced in the second quarter of 2003 with production shipments beginning in the quarter ended September 27, 2003.

Revenues by geographic region for the nine months ended September 27, 2003 as a percentage of revenues were 56.5% in North America, 9.1% in Europe, 18.7% in Asia Pacific and 15.7% in Japan. Revenues by geographic region for the nine months ended September 28, 2002 as a percentage of revenues were 58.4% in North America, 14.0% in Europe, 21.7% in Asia Pacific and 5.9% in Japan. For the nine months ended September 27, 2003, revenues for all geographic regions except Europe increased due to strong demand for our products. Revenues for Europe declined due to decreased revenues from a manufacturer of DRAM devices driven by the timing of tooling events at that customer.

The following customers accounted for more than 10% of our revenues for the nine months ended September 28, 2002 or September 27, 2003:

	Nine Months Ended	
	September 28, 2002	**September 27, 2003**
Intel Corporation	27.0%	34.6%
Spirox Corporation	20.8	15.1
Samsung Electronics Industries Co., Ltd.	*	10.8
Infineon Technologies AG	19.9	*
Micron Technologies, Inc.	10.8	*

*Less than 10% of revenues.

Gross Margin. Gross margin as a percentage of revenues was 48.4% for the nine months ended September 27, 2003 compared with 49.5% for the nine months ended September 28, 2002. The decrease in gross margin percentage was primarily due to increased investment in quality systems, manufacturing processes and procedures and the costs necessary to increase capacity. We increased our manufacturing fixed costs in response to continued positive demand for our products and continued design wins. This investment, primarily in headcount, was essential to convert our operations to a 7 day, 24 hour manufacturing shift structure which began in the second quarter of 2003 and was completed in the third quarter of 2003. This manufacturing structure increased our capacity and supports the first steps in establishing the required staffing levels to transfer our manufacturing processes into our new production facility in 2004.

Research and Development. Research and development expenses increased to $11.3 million, or 16.9% of revenues, for the nine months ended September 27, 2003 compared to $10.7 million, or 18.9% of revenues, for the nine months ended September 28, 2002. The increase in absolute dollars was primarily due to increased personnel costs reflecting our commitment to the development of new products and technologies. During the nine months ended September 27, 2003, we continued our development of fine pitch memory and logic products, advanced MicroSpring interconnect technology and new manufacturing process technologies.

Selling, General and Administrative. Selling, general and administrative expenses were $13.5 million for the nine months ended September 27, 2003 compared to $12.4 million for the nine months ended September 28, 2002. Selling, general and administrative expenses as a percentage of revenues were 20.2% and 22.0% for the

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first nine months of 2003 and 2002, respectively. The increase in absolute dollars was mainly due to increased personnel costs, higher sales and marketing spending, in line with higher revenues and new product introductions, and costs associated with being a public company.

Interest and Other Income (Expense), Net. Interest and other income (expense), net for the nine months ended September 27, 2003 was $780,000 compared with $404,000 for the nine months ended September 28, 2002. We generated greater interest income in the first nine months of 2003 due to a larger cash and cash equivalents balance as a result of our initial public offering in the second quarter of 2003. In addition, the increased business in Japan combined with the weaker dollar generated foreign currency gains for the first nine months of fiscal 2003 compared to foreign currency losses for the first nine months of fiscal 2002.

Benefit (Provision) for Income Taxes. Provision for income taxes was $2.8 million for the nine months ended September 27, 2003 compared to a benefit of $4.2 million for the nine months ended September 28, 2002. The provision for the nine month period ended September 27, 2003 reflected an effective tax rate of 38%. The $4.2 million benefit for the nine month period ended September 28, 2002 resulted from the release of the valuation allowance against our deferred tax assets in the amount of $5.9 million in the third quarter of 2002.

Fiscal Years Ended December 28, 2002 and December 29, 2001

Revenues. Revenues were $78.7 million for fiscal 2002 compared with $73.4 million for fiscal 2001, an increase of 7.2%. The $5.3 million increase was due primarily to an increase of $3.7 million in revenues from manufacturers of flash memory devices and an increase of $3.5 million in revenues from a manufacturer of chipsets, offset in part by a reduction of $1.6 million in revenues from DRAM manufacturers.

In fiscal 2001, we introduced our wafer probe cards to manufacturers of flash memory devices. The design wins and penetration at these customers, combined with increased demand for dense flash devices, generated the increased flash memory device related revenues in fiscal 2002.

The industry trend of faster and smaller devices resulting in increased power handling requirements has caused large scale integrated logic devices to migrate from wirebond-based package technologies to flip chip packaging. Our capabilities in flip chip microprocessor wafer probe cards enabled us to qualify and sell our wafer probe cards for chipset device probing applications, such as memory controller integrated circuits, in fiscal 2002. We generated minimal revenue from sales to chipset device manufacturers in fiscal 2001.

Consistent with fiscal 2001, the majority of fiscal 2002 revenues were generated by sales of wafer probe cards to manufacturers of DRAM devices. The decrease in revenues from DRAM manufacturers in fiscal 2002 was due primarily to reduced design activity and weaker bit growth. In addition, sales of Rambus DRAM, or RDRAM, wafer probe cards declined in fiscal 2002 compared to fiscal 2001. During the first two quarters of fiscal 2001, parts of the semiconductor industry adopted RDRAM architecture-based memory devices for higher speed applications. This adoption drove increased design activity and demand for wafer probe cards. During the second half of fiscal 2001, demand for Rambus-based chipsets and RDRAM devices decreased, a trend that persisted through fiscal 2002. This resulted in declining overall sales due to a significant decline in demand for RDRAM wafer probe cards. For fiscal 2002, our sales of RDRAM wafer probe cards decreased by $8.7 million compared to fiscal 2001 while sales of other DRAM wafer probe cards increased by $7.1 million. The increase in our other DRAM wafer probe card revenues was primarily the result of increased sales of our DRAM large area array wafer probe cards and the industry s conversion to DDR based DRAM devices in the second half of fiscal 2002.

Revenues by geographic region for fiscal 2002 as a percentage of total revenues were 55.6% in North America, 15.5% in Europe, 21.8% in Asia Pacific and 7.1% in Japan. Revenues by geographical region for fiscal 2001 as a percentage of total revenues were 52.7% in North America, 13.8% in Europe, 26.6% in Asia Pacific and 6.9% in Japan. The increase in the percentage of revenues in North America was due primarily to increased sales to a manufacturer of flash memory and chipset devices. The decrease in percentage of revenues in Asia Pacific was due primarily to decreased sales to our distributor of DRAM wafer probe cards.

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The following customers accounted for 10% or more of our revenues in fiscal 2001 or fiscal 2002:

	Fiscal 2001	Fiscal 2002
Intel Corporation	12.4%	26.9%
Spirox Corporation	26.4	20.9
Infineon Technologies AG	16.1	20.1
Samsung Electronics Industries Co., Ltd.	20.2	*

* Less than 10% of revenues.

The increase in revenues from certain of these customers for fiscal 2002 resulted from increased sales of microprocessor and flash memory wafer probe cards to one of these customers and increased sales of large area array DRAM devices to another one of these customers. In fiscal 2002, sales to certain customers were negatively impacted by an overall decreased demand for DRAM wafer probe cards.

Gross Margin. Gross margin as a percentage of revenues was 49.9% for fiscal 2002 compared with 47.7% for fiscal 2001. The increase in gross margin percentage was primarily due to cost reduction actions associated with our restructuring in the third quarter of fiscal 2001, continued reductions in the cost of materials, and shipments of high complexity products incorporating newer technology. These benefits were partially offset by a generally less favorable pricing environment due to the overall decline in demand. We also experienced an increase in warranty expenses caused primarily by an increase in field failures at one of our customers. Gross margin in absolute dollars and as a percentage of revenues will be subject to fluctuations as we continue to introduce new technologies into our manufacturing processes and to experience cyclicality in our end markets. We expect to continue to invest in new infrastructure, increasing fixed costs, which could have a material adverse impact on our gross margin.

Research and Development. Research and development expenses remained flat at $14.6 million, equivalent to 18.6% of revenues for fiscal 2002 compared to 19.9% of revenues for fiscal 2001. Personnel costs for fiscal 2002 increased by approximately $230,000 from fiscal 2001 and were partially offset by a reduction of approximately $175,000 for development program materials and related costs. During the first half of fiscal 2001, we completed the development of our MicroSpring Contact on Silicon Technology, or MOST technology. During the second half of fiscal 2001, we reduced spending while focusing our research and development efforts on developing wafer probe card products. Through fiscal 2002, we continued our development of new large area array memory products and fine pitch logic products.

Selling, General and Administrative. Selling, general and administrative expenses decreased to $17.0 million, or 21.6% of revenues, for fiscal 2002 compared to $18.5 million, or 25.2% of revenues, for fiscal 2001. The decrease was due primarily to a reduction of approximately $611,000 in personnel and recruiting costs and a reduction of approximately $752,000 in advertising, tradeshow and travel related expenses resulting from cost reduction actions taken in the second half of fiscal 2001.

Restructuring Charges. During the third quarter of fiscal 2001, we recorded a restructuring charge of $1.4 million. We implemented the restructuring plan to better align our infrastructure with the market conditions in the semiconductor industry and to further focus the company on the wafer probe card business. The restructuring charge consisted of $880,000 for headcount reductions covering 14 employees in research and development, 23 employees in operations and 17 employees in selling, general and administrative. The majority of the affected employees were based in Livermore, California. Further, we recorded charges of $223,000 for the consolidation of excess facilities and $277,000 for asset write-offs, primarily for property and equipment. The consolidation of excess facilities included the closure of certain corporate facilities that had been vacated. The charge of $223,000 primarily related to lease termination and noncancelable lease costs. The charge of $277,000 primarily related to the disposal of property and equipment, which primarily consisted of leasehold improvements for the excess facilities. As of December 28, 2002, the restructuring plan had been fully executed.

Interest and Other Income, Net. Interest and other income, net for fiscal 2002 was $642,000 compared to $477,000 for fiscal 2001, reflecting lower currency losses from the revaluation and translation of certain receivables and assets denominated in foreign currencies.

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Benefit (Provision) for Income Taxes. We recorded a benefit for income taxes for fiscal 2002 of $3.1 million compared to the provision of $307,000 for fiscal 2001. The benefit resulted from the release of the valuation allowance recorded against deferred tax assets, partially offset by the provision for income taxes on pre-tax profits. The valuation allowance was released because we believe that it is more likely than not that the deferred tax assets will be realized.

Fiscal Years Ended December 29, 2001 and December 30, 2000

Revenues. Revenues were $73.4 million for fiscal 2001 compared with $56.4 million for fiscal 2000, an increase of 30.2%. The increase was due to strong demand for our wafer probe cards used to test DRAM and flash memory devices. The increase in revenues reflected an increase in unit shipments, which was partially offset by a decline in average selling prices.

The increase of DRAM production, in particular RDRAM, at some of our customers impacted revenue growth favorably through the first six months of fiscal 2001. Revenues for this period also benefited from the introduction of our large area array products that enable a higher level of parallelism for test of memory devices. During fiscal 2001, we introduced our products to manufacturers of flash memory, which also contributed to our revenue growth.

During the second six months of fiscal 2001, our revenues declined compared to the first six months of fiscal 2001 as DRAM manufacturers experienced significant price declines for their products. This decline adversely impacted both the volume and pricing of our products. The effects of this decline were offset in part by increased demand for our products due primarily to technological innovations in the semiconductor industry, such as the migration toward smaller feature sizes of ..15 micron and below.

Revenues by geographic region in fiscal 2001 as a percentage of total revenues were 52.7% in North America, 13.8% in Europe, 26.6% in Asia Pacific and 6.9% in Japan. Revenues by geographic region in fiscal 2000 as a percentage of total revenues were 42.0% in North America, 16.4% in Europe, 33.4% in Asia Pacific and 8.2% in Japan. The year-to-year increase in revenues in North America was primarily due to the increased sales of RDRAMs by one of our major customers.

The following customers accounted for 10% or more of our revenues in fiscal 2000 or fiscal 2001:

	Fiscal 2000	Fiscal 2001
Spirox Corporation	25.4%	26.4%
Samsung Electronics Industries Co., Ltd.	*	20.2
Infineon Technologies AG	21.3	16.1
Intel Corporation	16.5	12.4

* Less than 10% of revenues.

Revenues to our largest customers during fiscal 2001 increased due to the ramp of RDRAM wafer probe products and the continued penetration of new end customers by our distributor Spirox. Revenue percentages declined for some of our customers due to our overall increased revenues during fiscal 2001, while revenues in absolute dollars to such customers remained flat.

Gross Margin. Gross margin as a percentage of revenues was 47.7% for fiscal 2001 compared with 49.9% for fiscal 2000. The decline in gross margin percentage was due to the overall industry downturn in the second half of fiscal 2001, resulting in increased pricing pressure and reduced unit volumes. Furthermore, we continued to incur start-up costs from the transition to a new manufacturing process for our next generation MicroSpring technology, which added new shapes and/or materials for our MicroSpring contacts and increased the amount of wafer fabrication-based processing, during the first six months of fiscal 2001. The start-up costs related to increased materials spending from pre-production lots, as well as reduced yields during the process ramp. Cost of revenues increased in fiscal 2001 due to continued investments in our manufacturing infrastructure, primarily increased personnel expenses, which impacted our gross margin unfavorably.

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Research and Development. Research and development expenses increased to $14.6 million, or 19.9% of revenues, for fiscal 2001 from $12.0 million, or 21.3% of revenues, for fiscal 2000. Of this increase, approximately $1.6 million was due to increases in headcount and approximately $480,000 was due to increased spending on engineering materials. This increased investment resulted in the development of large area array products and process technologies to enhance the manufacturability of various products. We also increased our investment in design capability to address a growing business in Asian markets.

Selling, General and Administrative. Selling, general and administrative expenses increased to $18.5 million, or 25.2% of revenues, for fiscal 2001 from $15.4 million, or 27.4% of revenues, for fiscal 2000. The increase was due to hiring additional personnel in sales, field applications and administrative capacities as well as increases in commissions due to increased revenues.

Restructuring Charges. During the third quarter of fiscal 2001, we recorded a restructuring charge of $1.4 million. We implemented the restructuring plan to better align our infrastructure with the market conditions in the semiconductor industry and to further focus the company on the wafer probe card business. The restructuring charge consisted of $880,000 for headcount reductions covering 14 employees in research and development, 23 employees in operations and 17 employees in selling, general and administrative. The majority of the affected employees were based in Livermore, California. Further, we recorded $223,000 for the consolidation of excess facilities and $277,000 for asset write-offs, primarily for property and equipment. The consolidation of excess facilities included the closure of certain corporate facilities that had been vacated. The charge of $223,000 primarily related to lease termination and noncancelable lease costs. Property and equipment that was disposed of resulted in a charge of $277,000 and primarily consisted of leasehold improvements for the excess facilities. As a result of our restructuring plan, we expect an annual reduction of employee related costs of $3.9 million and facility and related expenses of $266,000. As of December 29, 2001, $441,000 of the $1.4 million restructuring charge remained accrued, primarily relating to ongoing scheduled severance payments and pending lease contract cancellations being executed under the restructuring plan. We substantially completed these restructuring payment obligations as of the end of the third quarter of fiscal 2002.

Interest and Other Income, Net. Interest and other income, net for fiscal 2001 was $477,000 compared with $1.7 million for fiscal 2000. The difference was due to non-recurring other income of $1.3 million recorded in fiscal 2000 from the settlement of a claim against a licensee for an alleged breach of a license agreement.

Provision for Income Taxes. Provision for income taxes was $307,000 for fiscal 2001 compared with $115,000 for fiscal 2000. This increase represented the estimated tax liability for fiscal 2001 arising from both alternative minimum tax and income tax. As of December 29, 2001, our deferred tax asset was $9.1 million, representing prior years operating loss carry forwards and unutilized tax credits, and had been reduced in full by a valuation allowance.

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Quarterly Results of Operations

The following table presents our unaudited quarterly results of operations for the fifteen quarters in the period ended September 27, 2003. You should read the following table in conjunction with the consolidated financial statements and related notes contained elsewhere in this prospectus. We have prepared the unaudited information on the same basis as our audited consolidated financial statements. This table includes all adjustments, consisting only of normal recurring adjustments, that we consider necessary for a fair presentation of our financial position and operating results for the quarters presented. Operating results for any quarter are not necessarily indicative of results for any future quarters or for a full year.

	Three Months Ended														
	April 1, 2000	July 1, 2000	Sept. 30, 2000	Dec. 30, 2000	Mar. 31, 2001	June 30, 2001	Sept. 29, 2001	Dec. 29, 2001	Mar. 30, 2002	June 29, 2002	Sept. 28, 2002	Dec. 28, 2002	Mar. 29, 2003	June 28, 2003	Sept. 27, 2003
	(unaudited) (in thousands)														
Revenues	$10,313	$13,028	$15,842	$17,223	$19,849	$21,507	$16,021	$16,056	$17,288	$18,510	$20,729	$22,157	$18,669	$22,094	$26,076
Cost of revenues	5,198	6,159	7,808	9,078	10,410	11,269	8,477	8,229	8,859	9,422	10,259	10,916	9,800	11,469	13,213
Gross margin	5,115	6,869	8,034	8,145	9,439	10,238	7,544	7,827	8,429	9,088	10,470	11,241	8,869	10,625	12,863
Operating expenses:															
Research and development	2,516	2,699	3,247	3,533	4,073	4,323	3,054	3,169	3,249	3,579	3,828	3,936	3,525	3,831	3,966
Selling, general and administrative	2,904	3,500	4,431	4,599	4,730	5,230	4,344	4,196	3,992	4,172	4,265	4,576	4,013	4,478	4,980
Stock-based compensation	67	68	63	61	58	102	103	206	165	302	283	289	333	371	396
Restructuring charges							1,380								
Total operating expenses	5,487	6,267	7,741	8,193	8,861	9,655	8,881	7,571	7,406	8,053	8,376	8,801	7,871	8,680	9,342
Operating income (loss)	(372)	602	293	(48)	578	583	(1,337)	256	1,023	1,035	2,094	2,440	998	1,945	3,521
Interest and other income (expense), net	1,354	55	157	153	(74)	94	229	228	155	164	85	238	129	131	520
Income (loss) before income taxes	982	657	450	105	504	677	(1,108)	484	1,178	1,199	2,179	2,678	1,127	2,076	4,041
Benefit (provision) for income taxes	(51)	(34)	(24)	(6)	(207)	(291)	426	(235)	(332)	(485)	5,031	(1,089)	(428)	(789)	(1,536)
Net income (loss)	$ 931	$ 623	$ 426	$ 99	$ 297	$ 386	$ (682)	$ 249	$ 846	$ 714	$ 7,210	$ 1,589	$ 699	$ 1,287	$ 2,505

Net income (loss) per share:																								
Basic	$ .29	$ .19	$ .12	$ .03	$ .08	$ .10	$ (.16)	$ .06	$ .19	$ .16	$ 1.61	$ .35	$ .15	$ .12	$ .07									
Diluted	$ .03	$ .02	$ .02	$	$ .01	$ .01	$ (.16)	$ .01	$ .03	$ .02	$ .24	$ .05	$ .02	$ .04	$ .07									
Weighted-average number of shares used in per share calculations:																								
Basic	3,181	3,337	3,497	3,611	3,790	3,941	4,137	4,248	4,391	4,438	4,478	4,529	4,539	10,894	34,117									
Diluted	26,656	26,582	27,293	27,636	27,924	28,353	4,137	29,038	29,823	29,535	29,575	29,227	29,266	31,170	37,905									

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The following table presents our historical results for the periods indicated as a percentage of revenues:

	Three Months Ended														
	April 1, 2000	July 1, 2000	Sept. 30, 2000	Dec. 30, 2000	Mar. 31, 2001	June 30, 2001	Sept. 29, 2001	Dec. 29, 2001	Mar. 30, 2002	June 29, 2002	Sept. 28, 2002	Dec. 28, 2002	Mar. 29, 2003	June 28, 2003	Sept. 27, 2003
Revenues	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%
Cost of revenues	50.4	47.3	49.3	52.7	52.4	52.4	52.9	51.3	51.2	50.9	49.5	49.3	52.5	51.9	50.7
Gross margin	49.6	52.7	50.7	47.3	47.6	47.6	47.1	48.7	48.8	49.1	50.5	50.7	47.5	48.1	49.3
Operating expenses:															
Research and development	24.4	20.7	20.5	20.5	20.5	20.1	19.1	19.7	18.8	19.3	18.5	17.8	18.9	17.3	15.2
Selling, general and administrative	28.2	26.9	28.0	26.7	23.9	24.3	27.1	26.1	23.1	22.6	20.6	20.6	21.5	20.3	19.1
Stock-based compensation	0.6	0.5	0.4	0.4	0.3	0.5	0.6	1.3	1.0	1.6	1.3	1.2	1.8	1.7	1.5
Restructuring charges							8.6								
Total operating expenses	53.2	48.1	48.9	47.6	44.7	44.9	55.4	47.1	42.9	43.5	40.4	39.6	42.2	39.3	35.8
Operating income (loss)	(3.6)	4.6	1.8	(0.3)	2.9	2.7	(8.3)	1.6	5.9	5.6	10.1	11.1	5.3	8.8	13.5
Interest and other income (expense), net	13.1	0.4	1.0	0.9	(0.4)	0.4	1.4	1.4	0.9	0.9	0.4	1.0	0.7	0.6	2.0
Income (loss) before income taxes	9.5	5.0	2.8	0.6	2.5	3.1	(6.9)	3.0	6.8	6.5	10.5	12.1	6.0	9.4	15.5
Benefit (provision) for income taxes	(0.5)	(0.2)	(0.1)		(1.0)	(1.3)	2.6	(1.5)	(1.9)	(2.6)	24.3	(4.9)	(2.3)	(3.6)	(5.9)
Net income (loss)	9.0%	4.8%	2.7%	0.6%	1.5%	1.8%	(4.3)%	1.5%	4.9%	3.9%	34.8%	7.2%	3.7%	5.8%	9.6%

Revenues. Revenues increased sequentially in each of the quarters ended April 1, 2000 through June 30, 2001, due to increased demand across all markets for our wafer probe cards. Revenues declined during the three months ended September 29, 2001 due to the overall industry downturn, which resulted in a decline in unit volumes and pricing for our products. Revenues increased sequentially in each of the quarters ended December 29, 2001 through December 28, 2002 as design activity increased, primarily in the DRAM, driven by the architecture conversion to DDR, and logic markets. Revenues for the quarter ended March 29, 2003 declined primarily due to the completion of the DDR tooling cycle and the resulting lower demand for DRAM wafer probe cards. Revenues for the quarters ended June 28, 2003 and September 27, 2003 increased due to increased demand for wafer probe cards to test flash memory devices.

Gross Margin. Gross margin by quarter increased to 52.7% in the three months ended July 1, 2000, due to an increase in sales of higher performance products in that quarter. Gross margin declined between the three months ended July 1, 2000 and the three months ended December 30, 2000, due to the start-up costs associated with a new manufacturing process as well as continued investments in our manufacturing infrastructure, primarily in increased personnel. Gross margin remained relatively stable from the three months ended December 30, 2000 through the three months ended September 29, 2001. Gross margin increased sequentially in each of the quarters ended December 29, 2001 through December 28, 2002 as a result of increased higher performance product sales and the benefits of our restructuring as well as other cost reduction programs, such as scheduled plant shutdowns. These benefits were partially offset by the overall industry downturn beginning in the second half of fiscal 2001 and continuing into 2002, resulting in increased pricing pressure. Gross margin decreased in the three months ended March 29, 2003 due to the increased investment in quality systems, processes and procedures and the cost of increased capacity. Gross margin for the quarters ended June 28, 2003 and September 27, 2003 increased due to increased revenues from higher performance products in that quarter.

Operating Expenses. Operating expenses increased in absolute dollars in each of the six quarters ended April 1, 2000 through June 30, 2001, reflecting the combination of increased staffing in all departments to support our overall business growth; increased spending on research and development to continue to develop new technologies for current and new applications; increased selling costs related to higher revenue levels; and increased management and infrastructure spending to support our planned growth and penetration into new markets. Operating expenses decreased in the three months ended September 29, 2001 and the three months

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ended December 29, 2001 as we restructured our operations in response to the overall industry downturn. Operating expenses continued to decline in the three months ended March 30, 2002, due to realization of ongoing benefits of our restructuring plan and further reduction of workforce during the three months ended December 29, 2001, and a scheduled plant shutdown. Operating expenses increased in each of the following three quarters due to the operation of plants that experienced periodic shutdowns in prior periods, increased research and development spending on new technologies and increased expenses related to increased revenues. Operating expenses declined for the three months ended March 29, 2003 as spending was reduced in response to the lower revenue level. Operating expenses for the quarters ended June 28, 2003 and September 27, 2003 increased due to higher sales and marketing spending, in line with our higher revenues and costs associated with being a public company.

Our quarterly operating results are likely to fluctuate, and if we fail to meet or exceed the expectations of securities analysts or investors, the trading price of our common stock could decline. Some of the important factors that could cause our revenues and operating results to fluctuate from period-to-period include:

customer demand for our products;

our ability to deliver reliable, cost-effective products in a timely manner;

the reduction, rescheduling or cancellation of orders by our customers;

the timing and success of new product introductions and new technologies by our competitors and us;

our product and customer sales mix and geographical sales mix;

changes in the level of our operating expenses needed to support our anticipated growth;

a reduction in the price or the profitability of our products;

changes in our production capacity or the availability or the cost of components and materials;

our ability to bring new products into volume production efficiently;

the timing of and return on our investments in research and development;

our ability to collect accounts receivable;

seasonality, principally due to our customers purchasing cycles; and

market conditions in our industry, the semiconductor industry and the economy as a whole.

The occurrence of one or more of these factors might cause our operating results to vary widely. As such, we believe that period-to-period comparisons of our revenues and operating results are not necessarily meaningful and should not be relied upon as indications of future performance.

Critical Accounting Policies and Estimates

We believe the following critical accounting policies affect our more significant judgments and estimates used in the preparation of our consolidated financial statements.

Revenue Recognition. We recognize revenue in accordance with Securities and Exchange Commission Staff Accounting Bulletin No. 101, Revenue Recognition in Financial Statements, as amended by SAB 101A and 101B. SAB 101 requires that four basic criteria must be met before revenue can be recognized: (1) persuasive evidence of an arrangement exists; (2) delivery has occurred or services have been rendered; (3) the fee is fixed and determinable; and (4) collectibility is reasonably assured. Determination of criteria (3) and (4) are based on management s judgments regarding the fixed nature of the fee charged for services rendered and products delivered and the collectibility of those fees. Should

changes in conditions cause management to determine these criteria are not met for certain future transactions, revenue recognized for any reporting period could be adversely affected.

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Revenues from product sales to customers other than distributors are recognized upon shipment and reserves are provided for estimated allowances. We defer recognition of revenues on sales to distributors until the distributor confirms an order from its customer. Revenues from licensing of our design and manufacturing technology, which have been insignificant to date, are recognized over the term of the license agreement or when the significant contractual obligations have been fulfilled.

Accounts Receivable. We perform ongoing credit evaluations of our customers and adjust credit limits based upon payment history and the customer s current credit worthiness, as determined by our review of their current credit information. We continuously monitor collections and payments from our customers and maintain an allowance for doubtful accounts based upon our historical experience and any specific customer collection issues that we have identified. While our credit losses have historically been within our expectations and the allowance established, we might not continue to experience the same credit loss rates that we have in the past. Our accounts receivable are concentrated in a relatively few number of customers. Therefore, a significant change in the liquidity or financial position of any one customer could make it more difficult for us to collect our accounts receivable and require us to increase our allowance for doubtful accounts.

Warranty Reserve. We provide for the estimated cost of product warranties at the time revenue is recognized. While we engage in extensive product quality programs and processes, including actively monitoring and evaluating the quality of our component suppliers, our warranty obligation is affected by product failure rates, material usage and service delivery costs incurred in correcting a product failure. We continuously monitor product returns for warranty and maintain a reserve for the related expenses based upon our historical experience and any specifically identified field failures. As we sell new products to our customers, we must exercise considerable judgment in estimating the expected failure rates. This estimating process is based on historical experience of similar products as well as various other assumptions that we believe to be reasonable under the circumstances. Should actual product failure rates, material usage or service delivery costs differ from our estimates, revisions to the estimated warranty liability would be required.

From time to time, we may be subject to additional costs related to warranty claims from our customers. If and when this occurs, we generally make significant judgments and estimates in establishing the related warranty liability. This estimating process is based on historical experience, communication with our customers, and various assumptions that we believe to be reasonable under the circumstances. This additional warranty would be recorded in the determination of net income in the period in which the additional cost was identified.

Inventory Reserve. We state our inventories at the lower of cost, computed on a first in, first out basis, or market. We record inventory reserve for estimated obsolescence or unmarketable inventories equal to the difference between the cost of inventories and the estimated market value based upon assumptions about future demand and market conditions. If actual market conditions are less favorable than those projected by management, additional inventory reserve may be required.

Accounting for Income Taxes. We account for income taxes under the provisions of Statement of Financial Accounting Standards, or SFAS, No. 109, Accounting for Income Taxes. Under this method, we determine deferred tax assets and liabilities based upon the difference between the financial statement and tax bases of assets and liabilities using enacted tax rates in effect for the year in which the differences are expected to affect taxable income. The tax consequences of most events recognized in the current year s financial statements are included in determining income taxes currently payable. However, because tax laws and financial accounting standards differ in their recognition and measurement of assets, liabilities, equity, revenue, expenses, gains and losses, differences arise between the amount of taxable income and pretax financial income for a year and between the tax bases of assets or liabilities and their reported amounts in the financial statements. Because it is assumed that the reported amounts of assets and liabilities will be recovered and settled, respectively, a difference between the tax basis of an asset or a liability and its reported amount in the balance sheet will result in a taxable or a deductible amount in some future years when the related liabilities are settled or the reported amounts of the assets are recovered, hence giving rise to a deferred tax asset. We must then assess the likelihood that our deferred tax assets will be recovered from future taxable income and to the extent we believe that recovery is not likely, we must establish a valuation allowance.

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As of December 29, 2001, we had recorded a full valuation allowance of $9.1 million against our deferred tax assets, due to uncertainties related to our ability to utilize our deferred tax assets, primarily consisting of certain net operating losses carried forward, before they expire. In fiscal 2002, we released our valuation allowance because, based upon our recurring level of profitability, we believe that it is more likely than not that we will be able to utilize our deferred tax assets before they expire.

As part of the process of preparing our consolidated financial statements, we are required to estimate our income taxes. This process involves estimating our actual current tax exposure together with assessing temporary differences that may result in deferred tax assets. Management judgment is required in determining any valuation allowance recorded against our net deferred tax assets. Any such valuation allowance would be based on our estimates of taxable income and the period over which our deferred tax assets would be recoverable. While management has considered future taxable income and ongoing prudent and feasible tax planning strategies in assessing the need for the valuation allowance, if we were to determine that we would be able to realize our deferred tax assets in the future, in excess of their net recorded amount, an adjustment to the deferred tax asset would increase income in the period that determination was made.

Liquidity and Capital Resources

As of September 27, 2003, we had $121.6 million in cash, cash equivalents, short-term and long-term investments and restricted cash, compared with $32.2 million as of September 28, 2002. We completed our initial public offering of 6,000,000 shares of our common stock on June 17, 2003 and we subsequently sold an additional 900,000 shares pursuant to the exercise of the underwriters over-allotment option. These sales resulted in net proceeds of approximately $82.2 million.

Net cash provided by operating activities was $6.9 million for the nine months ended September 27, 2003 compared with net cash provided by operating activities of $6.7 million for the nine months ended September 28, 2002. The increase in net cash provided by operations for the nine month period ended September 27, 2003 resulted primarily from an increase in the net income for the nine month period when adjusted for the non-cash adjustments to net income compared to the same nine month period of 2002. Net cash provided by operating activities for fiscal 2002, 2001 and 2000 was $12.9 million, $10.3 million and $935,000, respectively. For fiscal 2002, cash was provided through net income increased by non-cash expenses such as depreciation, amortization and stock-based compensation, offset in part by the release of the valuation allowance for the deferred tax asset. For fiscal 2001, cash was provided by a reduction in working capital, as well as from net income increased by non-cash expenses. In fiscal 2000, cash was provided by net income, increased by non-cash expenses, offset in part by an increase in working capital, primarily accounts receivable.

Accounts receivable increased by $3.8 million for the nine months ended September 27, 2003 due to an increase in worldwide sales and specifically to an increase in sales in Japan, which historically have longer payment terms. Accounts receivable remained flat for fiscal 2002, compared to a decline of $501,000 for fiscal 2001, reflecting lower days sales outstanding, and an increase of $7.9 million for fiscal 2000. The increase in fiscal 2000 was due to increased revenues.

For the nine months ended September 27, 2003, inventories increased by $5.9 million due to an increase in raw materials and work-in-process to support revenue growth. Inventories increased in fiscal 2002, 2001 and 2000 by $683,000, $522,000 and $3.1 million, respectively, to meet the expected increased demand for our products.

Accrued liabilities increased from $7.7 million in fiscal 2002 to $9.3 million for the nine month period ended September 27, 2003 due primarily to the increase in accrued income taxes. Accrued liabilities increased from $3.5 million in fiscal 2000 to $5.8 million in fiscal 2001 and to $7.7 million in fiscal 2002. The increase was due to the increase in accrued incentive bonuses as part of our shift to more variable compensation, and sales commissions as well as an increase in accrued warranty costs reflecting higher revenue levels.

Net cash used by investing activities was $21.3 million for the nine months ended September 27, 2003, compared to $11.8 million used for investing activities for the nine months ended September 28, 2002. Net cash used in investing activities was $7.5 million for fiscal 2002 and $11.6 million for fiscal 2001. In fiscal 2000, investing activities provided $4.2 million. Capital expenditures were $5.7 million for the nine months ended

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September 27, 2003 and $3.0 million for the nine months ended September 28, 2002. Capital expenditures were $4.2 million for fiscal 2002, $9.4 million for fiscal 2001 and $6.3 million for fiscal 2000. We invested in the expansion of manufacturing facilities as well as in leasehold improvements to our new headquarters and manufacturing facility. These capital expenditures were partially offset or increased by the net maturity or purchase of investments in each of these periods.

Net cash provided in financing activities was $83.2 million for the nine months ended September 27, 2003 compared with net cash provided by financing activities of $1.0 million for the nine months ended September 28, 2002. Net cash provided by financing activities was $863,000 for fiscal 2002, $10.0 million for fiscal 2001 and $2.5 million for fiscal 2000. Net cash provided by financing activities was primarily due to the issuance of common stock in fiscal 2002 and in the nine months ended September 27, 2003 and to the net sale of our redeemable convertible preferred stock in fiscal 2001 and fiscal 2000 partially offset by debt repayments in each of these periods. In June 2003, we completed our initial public offering and raised net proceeds of approximately $82.2 million.

In May 2001, we signed a ten-year lease for an additional 119,000 square feet of manufacturing, research and development and office space. The total rent obligation over the term of the lease is $21.8 million and is accounted for as an operating lease. Our obligations under our operating leases for fiscal 2003 were approximately $600,000 as of September 27, 2003. We expect to invest approximately $25.0 million in leasehold improvements for our new headquarters and manufacturing facility through the third quarter of 2004. Of this amount, approximately $18.0 million relates to the design and construction of a new manufacturing facility, while the remaining amount relates to the build out and infrastructure of research and development and office space.

In February 2003, we entered into an amended and restated loan and security agreement with Comerica Bank. Our loan and security agreement provides a revolving line of credit of up to $16.0 million. In April 2003, we borrowed funds under the revolving line of credit to pay down the outstanding amounts under the expiring equipment line of credit and term loan under our prior agreement with Comerica. At September 27, 2003, we had no outstanding amounts under this agreement and approximately $16.0 million was available for future borrowings. Borrowings under our loan and security agreement accrue interest based on either the Comerica Bank prime rate or the London Inter Bank Offered Rate, or LIBOR, plus 2.0%. The financial covenants in our agreement require us to maintain cash and cash equivalents of a minimum of $3.0 million, limit capital expenditures to a maximum of $30.0 million per fiscal year, and provide specific levels of profitability which we must achieve. As of September 27, 2003, we had complied with these and all other covenants in our agreement with Comerica Bank. Our loan and security agreement expires on October 30, 2004. We have no debt obligations that have not been recorded in our consolidated financial statements.

The following table describes our commitments to settle contractual obligations in cash as of September 27, 2003.

	Payments due by Fiscal Year				
	2003	2004-2005	2005-2007	After 2008	Total
			(in thousands)		
Operating leases	$792	$4,684	$4,516	$8,463	$18,455

We believe our existing cash balance and loan and security agreement will be sufficient to meet our anticipated cash needs for at least the next 12 months. Our future capital requirements will depend on many factors, including our rate of revenue growth, the timing and extent of spending to support product development efforts, the expansion of sales and marketing activities, the timing of introductions of new products and enhancement to existing products, the costs to ensure access to adequate manufacturing capacity, and the continuing market acceptance of our products. To the extent that funds generated by this offering, together with existing cash, cash equivalents and short-term and long-term investments and any cash from operations, are insufficient to fund our future activities, we may need to raise additional funds through public or private equity or debt financing. Although we are currently not a party to any agreement or letter of intent with respect to potential investments in, or acquisitions of, complementary businesses, products or technologies, we may enter into these

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types of arrangements in the future, which could also require us to seek additional equity or debt financing. Additional funds may not be available on terms favorable to us or at all.

Recent Accounting Pronouncements

In November 2002, the Emerging Issues Task Force, or EITF, reached a consensus on Issue No. 00-21, Revenue Arrangements with Multiple Deliverables. EITF Issue No. 00-21 provides guidance on how to account for arrangements that involve the delivery or performance of multiple products, services and/or rights to use assets. The provisions of EITF Issue No. 00-21 will apply to revenue arrangements entered into in fiscal periods beginning after June 15, 2003. We do not expect the adoption of EITF Issue No. 00-21 to have a material impact on our financial position or on our results of operations.

In January 2003, the FASB issued FASB Interpretation No. 46, or FIN 46, Consolidation of Variable Interest Entities, an Interpretation of ARB No. 51. FIN 46 requires certain variable interest entities to be consolidated by the primary beneficiary of the entity if the equity investors in the entity do not have the characteristics of a controlling financial interest or do not have sufficient equity at risk for the entity to finance its activities without additional subordinated financial support from other parties. FIN 46 was effective immediately for all new variable interest entities created or acquired after January 31, 2003. For variable interest entities created or acquired prior to February 1, 2003, the provisions of FIN 46 must be applied for the first interim or annual period beginning after June 15, 2003. In October 2003, the FASB deferred the implementation date by which all public companies must apply FIN 46. We must apply FIN 46 no later than the first reporting period ending after December 15, 2003. The FASB agreed to provide this deferral to allow time for certain implementation issues to be addressed through the issuance of a modification to FIN 46, and indicated that it expects to issue this modification in final form prior to the end of 2003. We do not expect the adoption of FIN 46 to have a material impact on our financial position or on our results of operations.

In April 2003, the FASB issued Statement No. 149 Amendment of Statement 133 on Derivative Instruments and Hedging Activities, or SFAS No. 149. SFAS No. 149 requires that contracts with comparable characteristics be accounted for similarly. In particular, SFAS No. 149 clarifies under what circumstances a contract with an initial net investment meets the characteristic of a derivative, clarifies when a derivative contains a financing component, amends the definition of an underlying to conform it to language used in FIN 45 Guarantor s Accounting and Disclosure Requirements for Guarantees, Including Indirect Guarantees of Indebtedness of Others , and amends certain other existing pronouncements. SFAS No. 149 is effective for contracts entered into or modified after June 30, 2003, and for hedging relationships designated after June 30, 2003. In addition, provisions of SFAS No. 149 should be applied prospectively. We do not expect the adoption of SFAS No. 149 to have a material impact on our financial position or on our results of operations.

In May 2003, the FASB issued Statement No. 150 Accounting for Certain Financial Instruments with Characteristics of both Liabilities and Equity, or SFAS No. 150. SFAS No. 150 establishes standards for how an issuer classifies and measures certain financial instruments with characteristics of both liabilities and equity. SFAS No. 150 requires that an issuer classify a financial instrument that is within its scope as a liability, or an asset in some circumstances. SFAS No. 150 is effective for financial instruments entered into or modified after May 31, 2003, and otherwise is effective at the beginning of the first interim period beginning after June 15, 2003. SFAS No. 150 is to be implemented by reporting the cumulative effect of a change in an accounting principle for financial instruments created before the issuance date of SFAS No. 150 and still existing at the beginning of the interim period of adoption. Restatement is not permitted. We do not expect that the adoption of SFAS No. 150 to have a material impact on our financial position or on our results of operations.

Quantitative and Qualitative Disclosure of Market Risks

Foreign Currency Exchange Risk. Our revenues, except in Japan, and our expenses, except those expenses related to our Germany, United Kingdom, Japan and Korea operations, are denominated in U.S. dollars. As a result, we have relatively little exposure for currency exchange risks and foreign exchange losses have been minimal to date. We do not currently enter into forward exchange contracts to hedge exposure denominated in foreign currencies or any other derivative financial instruments for trading or speculative purposes. In the future,

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if we feel our foreign currency exposure has increased, we may consider entering into hedging transactions to help mitigate that risk.

Interest Rate Risk. The primary objective of our investment activities is to preserve principal while at the same time maximizing the income we receive from our investments without significantly increasing risk. Some of the securities in which we invest may be subject to market risk. This means that a change in prevailing interest rates may cause the principal amount of the investment to fluctuate. For example, if we hold a security that was issued with an interest rate fixed at the then-prevailing rate and the prevailing interest rate later rises, the principal amount of our investment will probably decline. To minimize this risk in the future, we intend to maintain our portfolio of cash equivalents, and short-term and long-term investments in a variety of securities, including commercial paper, money market funds, government and non-government debt securities and certificates of deposit. The risk associated with fluctuating interest rates is limited to our investment portfolio and we do not believe that a 10% change in interest rates will have a significant impact on our interest income. As of September 27, 2003, all of our investments were in money market accounts, certificates of deposit or high quality corporate debt obligations and U.S. government securities.

Our exposure to market risk also relates to the increase or decrease in the amount of interest expense we must pay on our outstanding debt instruments, primarily borrowings under a financing agreement we entered into with a financial institution in March 2001. See Note 5 of the notes to our consolidated financial statements. As of September 27, 2003, this facility provides for borrowings up to $16.0 million, of which $16.0 million is available for future borrowings. At September 27, 2003, no amount was outstanding under this facility. The loans bear a variable interest rate based on either the Comerica Bank prime rate or the LIBOR plus 2%. The risk associated with fluctuating interest expense is limited to this debt instrument and we do not believe that a 10% change in the prime rate or LIBOR would have a significant impact on our interest expense.

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BUSINESS

Overview

We design, develop, manufacture, sell and support precision, high performance advanced semiconductor wafer probe cards. In 2002, we were the leader in the advanced wafer probe card market in terms of revenues. Our products are based on our proprietary MicroSpring interconnect technology. This technology, which includes resilient spring-like contact elements, enables us to produce wafer probe cards for applications that require reliability, speed, precision and signal integrity. We manufacture our MicroSpring contact elements through precision micro-machining and scalable semiconductor-like wafer fabrication processes. We offer our customers high parallelism, large area array wafer probe cards to reduce their overall cost of test. We believe that our customers will be able to use our technology to optimize the semiconductor manufacturing pipeline, from initial device design and fabrication through system assembly and test, by performing more advanced test functions on whole wafers in the front-end of the semiconductor manufacturing process, rather than on individual devices in the back-end.

We introduced our first wafer probe card based on our MicroSpring interconnect technology in 1995, and, by the end of 2000, we were the leading supplier of advanced wafer probe cards, based on revenues, according to VLSI Research, an independent research firm. Our customers include the top 10 dynamic random access memory, or DRAM, manufacturers, the world s largest microprocessor company, and four of the top 10 flash memory manufacturers; and, combined, these identified groups of our customers account for substantially all of our revenues. We focus our research and development activities on expanding our products into new markets and developing new applications for our MicroSpring interconnect technology. We manufacture our wafer probe cards in Livermore, California, and sell and support our products worldwide through our direct sales force, a distributor and independent sales representatives.

Industry Background

Integrated circuits, also commonly referred to as semiconductors, devices or chips, are complex electronic devices made up of a large number of transistors that are fabricated on wafers, packaged and integrated into systems used in a wide range of electronic products, including personal computers, portable electronics, telecommunication equipment, wireless applications and digital consumer electronics. The World Semiconductor Trade Statistics estimates that over 78.6 billion chips were shipped in 2002.

The Continual Evolution of the Chip Faster, Smaller, Lower Cost

The ability to integrate increasing numbers of transistors on a given area of silicon has allowed the semiconductor industry to manufacture faster, smaller and more complex devices at a decreasing cost. Over time, the complexity of semiconductors has increased significantly, with the number of transistors on a chip doubling approximately every 18 months, with an accompanying decrease in the cost per device. This evolutionary phenomenon was first articulated by Dr. Gordon Moore, a co-founder of Intel Corporation, and has come to be known as Moore s Law.

In order to satisfy the demand for faster, smaller and lower cost chips, the semiconductor industry continually develops manufacturing, process and design improvements, most recently including the following:

Smaller Geometries. The ability to reduce the feature sizes within transistors in a chip to .13 micron and below is enabling manufacturers to produce greater numbers of chips per wafer, or the same number of chips with greater complexity, improve performance and reduce cost.

300 mm Wafers. The transition of the standard wafer form factor from 200 mm to 300 mm will more than double the available area on a wafer, significantly increasing the number of chips per wafer and further reducing the cost at which chips can be manufactured.

Copper Interconnect. Because of copper s higher level of conductivity as compared to aluminum, the transition from aluminum to copper as the preferred wiring material for interconnecting layers within chips is enabling higher speeds and greater performance.

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Low-K and Super Low-K Dielectrics. The introduction of new insulating materials such as low-k and super low-k dielectrics will enable improved device performance by reducing signal delay and electrical cross-talk, or interference, between increasingly densely-packed electrical connections on a chip.

With these changes, the semiconductor industry is currently experiencing a critical technology evolution. This evolution is resulting in a substantial increase in the cost of building new manufacturing capacity, with the cost of a leading edge 300 mm wafer manufacturing facility now approaching or exceeding $3.0 billion. With ever increasing capital investments, semiconductor manufacturers are focusing on ways to accelerate their return on investment by increasing volumes and yields, decreasing manufacturing costs and improving the time to market of their products.

The Chip Manufacturing Front-End and Back-End Processes

The semiconductor industry has historically separated the manufacture of chips into two distinct parts: the front-end wafer fabrication process, and the back-end assembly, packaging and final test process. The front-end process involves numerous complex and repetitive processing steps, including deposition, photolithography, etch and ion implantation, during which hundreds or even thousands of copies of an integrated circuit are formed simultaneously on a single wafer. After fabrication of the wafer is complete, the wafer is subject to wafer probe test. During wafer probe test, a wafer probe card is mounted in a prober, which is in turn connected to a semiconductor tester, sends an electrical signal through each chip on the wafer and verifies whether the chip performs basic functions, such as sending and receiving electrical signals. In some instances, wafer probe test is also used for more in-depth testing of the performance of the chip against design specifications. All of the steps in the front-end process, including wafer probe test, are performed at the wafer-level, before the wafer is cut into individual chips.

After wafer probe test, the wafer is transferred to the back-end portion of the manufacturing process. The first step in the back-end process is singulation, in which the wafer is cut into individual die. As a result of this first step, all subsequent back-end process steps must be performed at the individual chip level and, therefore, cannot be performed with the economies of scale afforded by the whole-wafer steps of the front-end process. After singulation, die that failed wafer probe test are discarded and the remaining die are assembled and packaged. The packaged chips are then subjected to final test over a range of operating conditions and temperatures to confirm that the packaged chips perform according to full specifications. Chips are sorted by performance characteristics and those passing final test standards are ready to be incorporated into a system.

The following diagram depicts the typical design to system semiconductor manufacturing pipeline:

In view of the increasing complexity of semiconductor fabrication, manufacturers have introduced technologies to increase yields and minimize costs. In the front-end process, for example, manufacturers are using metrology and inspection tools to identify, diagnose and minimize fabrication defects. Manufacturers also perform parametric test to verify process uniformity and capability. These tools confirm compliance with some

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manufacturing criteria, but they cannot test the functional electrical performance of a chip and, therefore, cannot confirm whether chips perform according to specifications.

The Significance and Cost of Test

Test is a critical part of the manufacturing process. In addition to identifying chips that do not function properly, both wafer probe test and final test generate information that may be used to redesign the chip or to implement manufacturing process changes that can result in improved chip yield. Test is the only process step that semiconductor manufacturers perform during both the front-end and back-end processes, and the cost of test is high. According to Infrastructure, Inc., an independent market research firm, the price for a high-end tester for logic chips has increased 25-fold over the last two decades from about $400,000 per system in the 1980s, to $3.0 to $5.0 million in the mid-1990s, to $6.0 to $10.0 million today. In addition, according to the International Technology Roadmap for Semiconductors, the cost per pin of testing is expected to remain relatively constant in the near future, while the number of pins per chip is projected to grow by 10% per year, resulting in the cost of test becoming a larger portion of the overall cost of manufacturing a device.

One way to address the high cost of test is to migrate elements of test from the individual chip level of the back-end process to the whole-wafer level of the front-end process. If wafer probe test can be used to provide greater levels of device validation, manufacturers will expend less time and money in the back-end process assembling, packaging and testing defective chips. This test migration will also reduce manufacturers need to purchase more processing equipment and testers to handle increasingly complex chips and the increasing number of chips per wafer. However, the migration of elements of final test to the front-end process will place significant capability and performance demands on wafer probe test.

Wafer Probe Test

During wafer probe test, wafer probe cards are used as an interface to electrically connect with and test individual chips on a wafer by moving the wafer into contact with the wafer probe card. The contact that occurs between the wafer probe card and the input/output terminals, or bond pads, of the chips on the wafer is commonly called a touchdown. Some wafer probe cards are capable of contacting the bond pads of more than one chip on the wafer at a time. This capability is known as parallelism. Depending on the number of chips on the wafer, and the testing parallelism capability of the wafer probe card, wafer probe test requires a varying number of touchdowns. For example, in order to test a typical 200 mm DRAM wafer containing approximately 400 to 500 chips, a wafer probe card that tests 32 chips per touchdown could require 15 to 18 touchdowns, depending on the layout of the chips on the wafer. A wafer probe card that tests 16 chips per touchdown could require twice the number of touchdowns to test a whole wafer. An increase in touchdowns means that test requires more time to complete and the cost of test increases.

In order to pass wafer probe test, chips must perform within a range of tolerances established by the manufacturer. A wide range will typically result in a higher yield from the front-end process, but an increased number of failures at final test. A narrow range will typically reduce final test failures and the costs associated with assembling and packaging defective chips, but reduce revenue per wafer because otherwise sellable chips will be discarded after wafer probe test as a result of their being incorrectly identified as failing to meet basic performance requirements commonly referred to as false fails.

The accuracy of wafer probe test is a function of the accuracy of the wafer probe test systems, which consist of the semiconductor tester, the prober, and the wafer probe card. The wafer probe card is mounted within the prober, which also houses the wafers to be probed or tested. The wafers are placed on a platform or chuck in the prober and precisely aligned with the wafer probe card to permit the probes on the wafer probe card to touchdown on the bond pads of one or more die on the wafer. Once this contact is made, the semiconductor tester, which is connected to the wafer probe card and prober, transmits electrical signals through the wafer probe card to the individual die on the wafer. Signals are then returned back through the wafer probe card to the semiconductor tester for evaluation. The signal integrity of the electrical path in the wafer probe card is a critical element of overall test accuracy. As wafer probe test accuracy increases, manufacturers can reduce the range of tolerance within which a chip must perform and realize an increase in chip yield at final test without suffering an

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unacceptable loss of yield from false fails at wafer probe test. Accordingly, manufacturers expend considerable time and expense creating test methodologies that optimize wafer probe test systems and wafer probe cards. VLSI Research forecasts that the wafer probe test market, comprised of wafer probe test systems and wafer probe cards, will grow from $1.3 billion in 2002 to $2.3 billion in 2005. VLSI Research also projects that the wafer probe card portion of the overall wafer probe test market, including spares and service revenue, will grow from $401.8 million in 2002 to $615.4 million in 2005.

Wafer probe cards for testing DRAM, flash, logic and microprocessor chips vary in design depending upon the type and design of the chip to be tested, the number of chips on the wafer, and the testing strategy of the chip manufacturer, including the selected semiconductor tester and prober. For example, these factors will affect the layout of the contact elements, the electrical path design, the presence or absence of additional components, such as capacitors, resistors or active elements, and the tester interface on the wafer probe card.

Wafer probe card purchases are driven by chip design changes and growth in the number of units manufactured. Because every semiconductor design is unique, every new chip design requires the use of a new wafer probe card customized for that design. Design changes result both from implementation of ongoing improvements to the design and manufacturing process of current generation chips and from application of new technologies and processes, such as shrinking geometries and the introduction of copper interconnects and low-k and super low-k dielectrics. Many semiconductor manufacturers will also implement new chip designs in connection with the transition to 300 mm wafers. During industry upturns when manufacturers are increasing capacity, chip unit growth is the principal driver of wafer probe card demand. However, even in industry downturns, semiconductor manufacturers typically continue to introduce new products or modify the designs of existing products, requiring new wafer probe cards.

Conventional Wafer Probe Card Technologies

VLSI Research divides current probe card technologies into two principal categories: needle probe cards and advanced technology wafer probe cards. The manufacture of needle, or epoxy-ring, probe card technology, which has been in existence for over 30 years, involves the gluing of needles with epoxy in a ring and manually bending the needles, typically a few inches long, to the specifications of a wafer probe card design. Advanced technology wafer probe cards are generally used to test chips with a high number of input/output pins, to test a significant number of chips in parallel, and to perform high speed testing. Advanced technology wafer probe cards include vertical or buckling beam, or COBRA, technology and membrane technology. COBRA probe card technology, based upon technology first described in 1966, uses manually-built vertical beam probes, which are long, slightly curved, vertical wires that buckle slightly as they contact a wafer. Membrane technology, which was introduced in the mid-1980s, probes chips by pressing contact tips mounted on flexible membranes to the wafer. We refer to needle probe cards and advanced technology wafer probe cards using the COBRA and membrane technology as conventional wafer probe cards or technologies. VLSI Research also identifies a third technology category, tungsten probes, which do not have widespread application for the faster, smaller and lower cost chips being developed and manufactured by the semiconductor industry.

The Limitations of Conventional Wafer Probe Card Technologies

Conventional wafer probe card technologies are starting to face practical performance limits due to one or more of the following factors:

Lack of Parallelism Increases Cost. Shrinking geometries and the transition to 300 mm wafers increases the number of chips per wafer. This increase imposes significant challenges for manufacturers of conventional wafer probe cards. Unless the number of chips that a wafer probe card is able to contact in parallel increases in proportion to the increasing number of chips on a wafer, the economies of scale generated during the front-end fabrication process cannot be matched during wafer probe test. To meet the demand for higher parallelism and in order to make uniform contact with the chips on the wafer, wafer probe cards need to be manufactured with large area probe arrays that are precisely engineered in a single level plane, or planarized. Because some conventional wafer probe cards must be manufactured in part by hand, those cards cannot, without great difficulty, if at

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all, be manufactured with precisely planarized probe arrays that are large enough to meet parallelism demands. As a consequence, those cards cannot match the increasing efficiencies of the front-end fabrication process. The result is that the cost of test increases as a percentage of total manufacturing cost.

Poor Signal Integrity Lowers Yield. Due to the limitations of their electrical characteristics, many conventional wafer probe card technologies limit the degree to which the test environment can replicate the environment in which the chip will be packaged and used. These limitations become more pronounced as operating frequency increases. As a result, conventional wafer probe cards may report a significant number of false fails and the engineering effort to prevent chip yield loss per wafer becomes more difficult.

Manual Assembly Impairs Precision. The manufacture of certain conventional wafer probe cards requires the manual attachment of the probing contact elements. Needle probe cards require manual assembly and positioning, which inherently results in less precision and requires continual adjustment at the chip manufacturer s fabrication facility. This limitation is magnified as device geometries shrink and enable more complex chips with an increasing number of input/output pins. With the increasing number of pins, smaller bond pad sizes are needed to provide electrical connections for those pins, and bond pads must also be located closer to each other, which is referred to as reduced pitch. It will become increasingly difficult for some conventional wafer probe cards, such as those using COBRA technology, to provide predictable contact with bond pads under these circumstances.

Testing at Extreme Temperature Negatively Affects Performance. Wafer probe test is often performed both below and above room temperature in order to replicate the operating condition at which the chip is expected to fail. For the flash memory market in particular, manufacturers may need to test at temperature ranges from -40°C to +150°C for chips used in some consumer and automotive applications. As temperature ranges increase, the component materials for conventional wafer probe cards are subject to a greater range of expansion and contraction, which significantly increases the complexity of making accurate contact with the bond pad. This problem is exacerbated by increases in the size of the probe array, or the number of probing elements that contact the bond pads of the chips on the wafer, and by increases in the number of chips under test. These challenges have limited many conventional wafer probe cards to smaller probe array sizes.

High Contact Force Reduces Yield and Tester Uptime. As new materials such as low-k and super low-k dielectrics are introduced into the chip manufacturing process, the force with which the wafer probe card contacts the chips on the wafer becomes increasingly important. Many of these new materials are relatively fragile. In order to make contact, conventional wafer probe cards apply significant force on the bond pads, which can damage the underlying structure of the chips. The likelihood of damage increases as the number of contacts on the same bond pad increases. As a result, the wafer probe card can cause an otherwise fully-functional chip to become defective or can cause latent defects that may impact reliability. This significant contact force also frequently generates debris and contaminants on the bond pads or probe tips, which can impair the electrical contact. Impaired electrical contact can result in false fails and reduced production yield. In addition, the existence of debris and contaminants requires that manufacturers frequently clean the test equipment, resulting in reduced overall tester uptime and increased test costs.

While some conventional wafer probe cards address various performance limitations, no conventional technology resolves all of the performance issues adequately. In many cases, the features of conventional wafer probe cards that solve one or more of the performance limitations compromise the performance of the wafer probe card in other areas. For example, while needle probe cards can provide a fast design to product cycle time that is advantageous for certain wafer test applications and smaller wafer volume requirements, the manual assembly and positioning requirements of needle probe cards negatively impact their precision and ability to meet the demand for higher parallelism arising out of certain other wafer test requirements. As a result, conventional wafer probe card technologies fail to meet the industry s need to reduce test cost. These cost inefficiencies will be magnified by new developments in the front-end process, including shrinking geometries and the move to

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300 mm wafers. We believe that in order for the cost of test to keep pace with the decreases in front-end process per chip manufacturing costs, not only must the performance limitations of conventional wafer probe card technologies be resolved, but more of the test functions must be performed at the wafer level. The semiconductor industry needs a solution that addresses the performance limitations of conventional wafer probe card technology and also enables the migration of more elements of final test to the front-end manufacturing process. Such a solution will help to better integrate the front-end and back-end processes and provides a scalable solution to the rising cost of test.

The FormFactor Solution

We design, develop, manufacture, sell and support precision, high performance advanced wafer test probe cards based on our proprietary MicroSpring interconnect technology. We believe that our wafer probe cards are the optimal test solution available today for probing chips at the wafer level and offer the potential for our customers to migrate elements of final test to wafer probe test.

Our wafer probe cards address the performance limitations of conventional wafer probe card technologies:

Our High Parallelism Advantage Reduces Cost of Test. Our high parallelism wafer probe cards enable our memory customers to test a significant number of chips in parallel in a single touchdown, reducing the cost of test and improving their time to market. Our wafer probe cards are manufactured with large probe arrays that are precisely planarized in order to contact uniformly the chips on the wafer. For example, our largest commercially available wafer probe cards can test most 200 mm DRAM wafers with as few as four touchdowns and most 300 mm DRAM wafers with as few as six touchdowns. This reduced number of touchdowns can significantly decrease total test time per wafer, resulting in a significant reduction in the cost of test.

Our High Signal Integrity Improves Yield. Due to the proprietary metallurgy and design of our wafer probe cards and our proprietary design processes, our wafer probe cards perform wafer probe test with a high level of signal integrity as compared to conventional needle cards. The signal measured at the tip of the MicroSpring contact element is reported to the wafer probe test system with a high degree of accuracy and with minimal signal loss and distortion. The result is that our wafer probe cards precisely measure the working performance of the chips and can operate with a flat or nearly flat response at higher frequencies. The precision of our measuring capability can improve wafer yields because our wafer probe cards generate fewer false fails during the wafer probe test. Our signal integrity also allows our customers to narrow their range of device test tolerances.

Precise MicroSpring Technology Enables Precise Probing. Our MicroSpring contact elements have geometrically precise contact tips that allow our customers to probe the increasingly small bond pad sizes and reduced pitches that chip manufacturers are implementing. We achieve this contact precision by manufacturing our wafer probe cards using micro-machining and semiconductor-like wafer fabrication processes, including deposition and photolithography. Because we employ some of the same processes used in front-end wafer fabrication, we are able to scale our testing capabilities to the shrinking geometries of semiconductors on a wafer. For example, our latest large area array platform is capable of precisely contacting in parallel 256 chips on a wafer having bond pads that measure 62 microns x 64 microns.

Compensation for Extreme Temperatures Improves Performance. The proprietary design of our wafer probe cards allows us to select materials and provide for precise matching of the thermal expansion characteristics of our wafer probe card with the wafer under test. As a result, our wafer probe cards generally are able to accurately probe over a large range of operating temperatures. Our current operating specification range is -40°C to +120°C. This feature enables our customers to use the same wafer probe card for both low and high temperature testing without a loss of performance. In addition, for those testing situations that require positional accuracy at a specific temperature, we have designed wafer probe cards optimized for testing at such temperatures.

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Lower Contact Force Increases Yield and Tester Uptime. Our MicroSpring contact elements have precise contact geometries, enabling the use of relatively low contact force during wafer probe test. Our proprietary technology allows us to implement spring elements having a spring constant of approximately one gram force per one-thousandth of an inch, or 1 gmf/mil, of deflection as compared to a range of 2 to 3 gmf/mil of deflection, to ensure stable, long-term contact performance. The lower contact force permitted by our technology allows our wafer probe cards to test chips incorporating fragile next-generation materials, such as low-k and super low-k dielectrics, without damaging the chips. As contact force decreases, our MicroSpring interconnect technology allows us to precisely design our contact tip geometries and materials to enable stable contact with current and future bond pad materials, such as copper. This lower contact force is also an advantage for probing solder bump wafers. With lower contact force, our wafer probe cards generate less debris when contacting the bond pads of the chips on the wafer, reducing false fails and reducing the need to clean our wafer probe cards, increasing uptime. This lower contact force, combined with the robust characteristics of our MicroSpring interconnect technology, provides our customers with a very durable and reliable probing solution. Our wafer probe cards also couple this lower contact force with a stable and consistent contact resistance over repeated touchdowns.

In addition to solving the limitations of conventional wafer probe cards, our MicroSpring interconnect technology and our other proprietary design tools and technology enable our customers to realize a lower total cost of test. Although we do not sell semiconductor testers or probers, our wafer probe cards can be designed to work in any manufacturer s wafer probe test system for DRAM, flash and flip chip logic devices. We believe that our existing technology enables us to test substantially all currently available DRAM, flash, logic and microprocessor devices, and substantially all emerging DRAM, flash and flip chip logic devices for which our customers have provided us designs or guidance. We employ a sales model that emphasizes the customer s total cost of ownership as it relates to test costs. We demonstrate how a customer s test costs can be reduced by simulating its test floor environment, including testers and probers, utilizing our products and comparing them to conventional wafer probe cards. We believe that the yield improvement, total cost of ownership and scalability advantages of our wafer probe cards, combined with our efforts to understand and solve our customers problems, allow us to capture a higher selling price compared to conventional wafer probe cards.

The migration of elements of final test from the packaged chip back-end process to front-end wafer probe test requires a wafer probe card technology that has a flat or nearly flat response at high frequencies along signal transmission lines, a minimal level of electrical cross-talk among signals, or interference, and a high degree of power decoupling, which minimizes power supply voltage variations at the chips being tested. We believe that the signal integrity of our wafer probe cards combined with their high parallelism and power decoupling characteristics meet these requirements and will facilitate the migration of elements of final test to front-end wafer probe test. We believe this migration will allow our customers to extend the benefits of wafer-level scaling to elements of final test and thereby enable them to feed back this test information earlier in the design and fabrication process, improving time to market. We believe that this migration will also enable our customers to realize a more cost effective, optimized semiconductor manufacturing pipeline.

Strategy

Our objectives are to enhance our position as the leading supplier of advanced wafer probe card solutions and to apply our MicroSpring interconnect technology to drive economies of scale at the wafer-level in semiconductor test. The principal elements of our strategy include:

Enhance our Market Leadership in the DRAM Industry. Our technology and products have enabled the DRAM industry to conduct high parallelism testing at the wafer level, with up to 253 chips under test in parallel. Parallelism is particularly important in the testing of DRAMs. As DRAM densities increase, test times also increase, because the time to test each cell within a chip is relatively fixed. Therefore, higher parallelism test is needed in order to maintain or improve the rate of throughput in test. We believe that in the future DRAM test will benefit by transitioning from high parallelism test to full wafer test in a single touchdown. To this end, we intend to work closely with our customers and business partners to deploy more highly parallel solutions which

are not commercially available, and ultimately a single touchdown solution for testing 200 mm and 300 mm DRAM wafers.

Expand our Presence in the Flash Memory Test Market by Leveraging our MicroSpring Interconnect Technology. The fundamental MicroSpring interconnect technology and large area array capabilities that enable high parallelism DRAM chip testing are transferable to flash memory testing, and we intend to continue to leverage into the flash memory test market the expertise and capabilities we have developed in the DRAM market. We successfully introduced in 2001 the industry s first high parallelism wafer probe cards for flash memory. Our existing commercially available technology is designed for flash memory tests up to 121 chips in parallel. We believe that our technology is capable of greater levels of parallelism, up to and beyond testing 144 chips in parallel. We intend to continue penetrating the flash memory test market, as we believe that flash memory will offer us additional growth opportunities outside of the personal computer-centric DRAM and microprocessor markets.

Increase our Penetration into the Logic Market. In the logic chip market, time to market is particularly critical, as significant market penetration requires very short lead times. As part of our strategy to address high volume applications, we have entered the microprocessor market. We believe that with increasing pin counts, an increasing number of logic applications will migrate toward large area array or flip chip packaging, which will create additional opportunities for the use of our products. Our wafer probe cards are also well suited for testing system on a chip, or SOC devices, where leading edge probe capability is required to meet a wide range of electrical, mechanical and temperature requirements. We are working with some of our customers to create custom wafer probe cards for testing SOC devices by addressing the specific pitch, parallelism, signal count, electrical integrity, current and test frequency requirements of customers SOC devices. We are also engaged in research and development activities directed to reducing our manufacturing costs and cycle time to compete more effectively, including in short lead time and lower volume wafer test applications.

Enable Migration of Elements of Final Test to the Wafer Level. We intend to continue to work with our customers to enable them to migrate elements of final test from the chip level to the wafer level. The benefits of obtaining test results earlier in the manufacturing process will become particularly important as the miniaturization of systems requires manufacturers to deliver fully functioning chips in die form, which increases the importance of having chips validated at the wafer level. For example, in the case of system in a package, or SIP, and small form factor applications, where unpackaged chips are included in a system, an individual chip that is not fully tested at the wafer level might cause the entire system to fail if the chip fails to deliver full performance. An important part of our strategy is to continue working with our customers to identify and implement programs in which our MicroSpring interconnect technology can help to migrate elements of final test to the front-end process.

Extend our Technology Leadership Position. With our MicroSpring interconnect technology, we have established a leading position in the advanced wafer probe card market. Wafer probe cards provide a rigorous and taxing environment for interconnection structures because they must touchdown on a wafer hundreds of thousands of times. Based on our success in developing wafer probe cards that can address these requirements, we believe that our MicroSpring interconnect technology can be applied in a broad range of applications where reliability, speed, precision and signal integrity are important, including wafer test, wafer-level packaging, final test, burn-in and socket and connector applications. We plan to continue to engage in research and development activities to extend our MicroSpring interconnect technology and other proprietary technologies to these and other applications.

Continue to Build on our Strategic Relationships. We have benefited from and plan to continue to rely on relationships with other industry participants. We have developed strategic relationships with leading semiconductor manufacturers and test equipment manufacturers. For example, we have engaged with tester companies, including Advantest Corporation, Agilent Technologies Inc. and Teradyne Inc., to introduce solutions that include wafer probe test systems and wafer probe cards. These engagements are typically informal in nature and have not historically been documented in written agreements. We have also engaged with semiconductor manufacturers to introduce new high parallelism test solutions and high frequency at-speed testing solutions. These engagements typically involve our designing and manufacturing of prototype probe cards for our customers. We believe these

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strategic relationships will facilitate faster product introduction and market acceptance for our customers and enhance our market position. Our strategic relationships also include licensing arrangements. We select applications for licensing, rather than manufacturing, where the applications are characterized by long adoption cycles, high barriers to entry, or the inclusion of our MicroSpring interconnect technology with one or more technologies that fall outside the area of our core competence.

FormFactor s MicroSpring Interconnect Technology and Products

Our products are based on our proprietary MicroSpring interconnect technology. Our MicroSpring contacts are springs that optimize the relative amounts of vertical contact force on, and horizontal force across, a bond pad during the test process and maintain their shape and position over a range of compression. These characteristics allow us to achieve reliable, electrical contact on either clean or oxidized surfaces, including bond pads on a wafer. Our MicroSpring contacts enable our wafer probe cards to make hundreds of thousands of touchdowns with minimal maintenance. The MicroSpring contact can be attached to many surfaces, or substrates, including printed circuit boards, silicon wafers, ceramics and various metalized surfaces. This flexibility allows the MicroSpring contact to be considered for use in a broad range of other applications, including chip scale packages, sockets and connectors.

Since its original conception, the MicroSpring contact has evolved into a library of spring shapes and technologies. Our designers use this library to design an optimized custom wafer probe card for each application. Since developing this fundamental technology, we have broadened and refined it to respond to the increasing demands of smaller, faster and more complex semiconductors. Our MicroSpring contacts have scaled in size with the evolution of semiconductors. Depicted in relative scale below are four of our basic spring types compared to a rendering of a standard No. 2 pencil.

Our MicroSpring contacts include geometrically precise tip structures. These tip structures are the parts of our wafer probe cards that contact the chips, and are manufactured using proprietary semiconductor-like processes. These tip structures enable precise contact with small bond pad sizes and pitches. Our technology allows us to specifically design the geometries of the contact tip in order to ensure the most precise and predictable electrical contact is achieved for a customer s particular application. We believe our technology will scale with that of front-end fabrication processes because we use proven semiconductor-like wafer fabrication processes and equipment in our manufacturing processes. As a consequence, we believe we have the ability to shrink wafer probe card contact geometries as necessary to test shrinking chip geometries on the wafer. However, because we do not use costly leading-edge equipment, we are able to manufacture in a less capital-intensive manner.

Our wafer probe cards are custom products that we design to order for our customers unique wafer designs. Contacting up to 256 chips in parallel requires large area contact array sizes because they must accommodate over 11,000 simultaneous contacts. This requirement poses fundamental challenges that include the planarity of the array, the force needed to make contact and the need to touch all bond pads with equal accuracy. We have developed wafer probe cards that use array sizes ranging from 50 mm x 50 mm to greater than 150 mm x

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150 mm, in combination with complex multi-layer printed circuit boards designed by our design team. While leading edge DRAM designs use larger array sizes for highly-parallel applications, smaller array sizes used for DRAM applications a few years ago can be used for today s leading edge applications in the flash memory and logic markets. Our current DRAM contacting technology allows our products to contact up to 256 DRAM chips in parallel. Our current flash contacting technology allows us to contact up to 144 flash chips in parallel. We believe that the levels of parallelism in our wafer probe cards that are produced in volume are one or two generations ahead of the volume production capabilities of our competitors.

We have invested and intend to continue to invest considerable resources in our wafer probe card design tools and process. These tools and processes enable automated routing and trace length adjustment within our printed circuit boards and greatly enhance our ability to rapidly design and lay out complex printed circuit board structures. Our proprietary design tools also enable us to design wafer probe cards particularly suited for testing today s low voltage, high power chips. Low voltage, high power chips require superior power supply performance, and our MicroSpring interconnect technology is used to provide a very low inductance, low resistance electrical path between the power source and the chip under test.

In July 2003, we publicly announced our MicroForce™ probing technology. Our MicroForce probing technology combines a low probe force with stable low resistance electrical contact to address wafer test challenges for high-performance, flip chip applications, thereby reducing the risk of damage to both interconnect bumps and the low-k dielectrics that lie beneath them. By combining our new BladeRunner MicroSpring contact structure with our proprietary technology directed to the automated wafer prober chuck, we believe our MicroForce probing technology will enable our customers to achieve a higher level of test accuracy, potentially increasing overall electrical yields by minimizing false failures. In July 2003, we also publicly announced our MicroLign™ alignment technology. Our MicroLign alignment technology includes a proprietary probe tip design method developed to optimize automated optical alignment during wafer probing. When implemented, this technology enables a faster, more accurate optical alignment process, which reduces instances of optical alignment errors and can drive manufacturing efficiencies for high volume wafer test operations.

Because our customers typically use our wafer probe cards in a wide range of operating temperatures, as opposed to conducting wafer probe test at one predetermined temperature, we have designed complex thermal compensation characteristics into our products. We select our wafer probe card materials after careful consideration of the potential range of test operating temperatures and design our wafer probe cards to provide for a precise match with the thermal expansion characteristics of the wafer under test. As a result, our wafer probe cards generally are able to accurately probe over a large range of operating temperatures. This feature enables our customers to use the same wafer probe card for both low and high temperature testing without a loss of performance. In addition, for those testing situations that require positional accuracy at a specific temperature, we have designed wafer probe cards optimized for testing at such temperatures.

Our many spring shapes, different geometrically-precise tip structures, various array sizes and diverse printed circuit board layouts enable a wide variety of solutions for our customers. Our designers select the most appropriate of these elements, or modify or improve upon such existing elements, and integrate them with our other technologies to deliver a custom solution optimized for the customer s requirements. We believe that the yield improvement, total cost of ownership and scalability advantages of our wafer probe cards, combined with our efforts to understand and solve our customers test problems, allow us to capture a higher selling price compared to conventional wafer probe cards.

Customers

Our customers include manufacturers in the DRAM, flash and logic markets. Our customers use our wafer probe cards to test DRAM chips including DDR, RDRAM, SDRAM and EDRAM, static RAM chips, NOR and NAND flash memory chips, Serial Data devices, chipsets, microprocessors and microcontrollers. Our DRAM customers include the 10 largest DRAM manufacturers in the world, and our flash customers include four of the 10 largest flash memory manufacturers in the world. We believe that our products are now used in more than 65

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wafer fabrication facilities worldwide. The table below is a representative list of semiconductor manufacturers that use our wafer probe cards:

DRAM Market	Flash Market
Elpida Memory, Inc.	Fujitsu AMD Semiconductor Ltd.
Hynix Semiconductor America, Inc.	Hitachi Nippon Steel
Infineon Technologies AG	Intel Corporation
Micron Technology, Inc.	Renesas Technology Corporation
Nanya Technology Corporation	Samsung Electronics Industries Co., Ltd.
PowerChip Semiconductor Corp.	Semiconductor Sing. Pte. Ltd.
ProMOS Technologies Inc.	
Samsung Electronics Industries Co., Ltd.	**Flip Chip Logic Market**
TECH Semiconductor Singapore Pte. Ltd.	Intel Corporation
Winbond Electronics Corporation	

In the nine months ended September 27, 2003, sales to three customers accounted for 60.5% of our revenues, with 34.6% attributable to Intel Corporation, 15.1% attributable to Spirox Corporation, our distributor, and 10.8% attributable to Samsung Electronics. In fiscal 2002, sales to three customers accounted for 67.9% of our revenues, with 26.9% attributable to Intel Corporation, 20.9% attributable to Spirox Corporation and 20.1% attributable to Infineon Technologies AG. In fiscal 2001, sales to four customers accounted for approximately 75.1% of our revenues, with 26.4% attributable to Spirox Corporation, 20.2% attributable to Samsung Electronics Industries Co., Ltd., 16.1% attributable to Infineon Technologies AG and 12.4% attributable to Intel Corporation. No other customer accounted for more than 10% of our revenues in any of these referenced periods.

Strategic Relationships and Licensees

We work closely with semiconductor tester manufacturers and prober manufacturers to maintain our leadership in advanced wafer probe test and to help our customers achieve faster product introduction and acceptance. For example, we worked with certain prober manufacturers to introduce our MicroForce probing and our MicroLign alignment technologies to the marketplace. We have also engaged with tester companies, including Advantest Corporation, Agilent Technologies Inc. and Teradyne Inc., to introduce complete test solutions for semiconductor manufacturers. These engagements are typically informal in nature and are not documented in written agreements. Thus, while we believe they are important to ensure the alignment of our product roadmaps with those of our customers, we have no contractual commitments or guarantees. We have also engaged with semiconductor manufacturers to introduce new high parallelism test solutions and high frequency at-speed testing solutions. These engagements typically involve our designing and manufacturing prototype wafer probe cards for our customers. We believe these relationships also serve to validate our basic test strategies and facilitate an integration of test and manufacturing roadmaps.

In 1998, we introduced a MicroSpring interconnect technology-based wafer level chip scale package using our proprietary MOST technology. MOST technology involves mounting MicroSpring contacts on the die on a wafer to be used both as the temporary connections necessary for test and as the permanent connections necessary to attach the chip to a separate component or module. MOST technology allows wafer level processing at the packaging step, providing customers a high performance, reliable, small footprint packaging solution. If customers combine our MOST technology with a wafer level test contactor, they can integrate the back-end assembly, packaging and final test process steps at the wafer level, allowing significant cost and performance advantages over traditional processing. We have also licensed our MOST technology for specific wafer-level packaging applications and our MicroSpring interconnect technology for incorporation into socket and connector applications.

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Sales and Marketing

We sell our products primarily through a sales model that emphasizes the customer s total cost of ownership as it relates to test costs. With this sales model, we strive to demonstrate how test costs can be reduced by simulating the customer s test floor environment, including testers and probers, utilizing our product and comparing the overall cost of test to that of conventional wafer probe cards.

We sell our products worldwide primarily through our direct sales force, a distributor and independent sales representatives. As of September 27, 2003, we had 19 sales professionals. In North America, we sell our products through our direct sales force. In Europe, our local sales team works with independent sales representatives. In South Korea, we sell our products through our direct sales force, while in Taiwan, China and Singapore we sell through Spirox Corporation, our distributor in the region. In Japan, effective April 1, 2002, we converted from a distributor arrangement to a direct sales team that is based in Tokyo, Japan.

Our marketing staff, located in Livermore, California and Tokyo, Japan, works closely with customers to understand their businesses, anticipate trends and define products that will provide significant technical and economic advantages to our customers.

We also utilize a highly skilled team of field application engineers that support our customers as they integrate our products into their manufacturing processes. Through this process, we develop a close understanding of product and customer requirements, speeding our customers production ramps. We plan to expand our customer support by adding engineering services. We believe this expanded service offering will enable our customers to more fully benefit from our products and technology and create new business opportunities for us.

Manufacturing

Our wafer probe cards are custom products that we design to order for our customers unique wafer designs. We manufacture our products at our facilities in Livermore, California. We believe that we are the first wafer probe card company to successfully utilize micro-machining and scalable semiconductor-like wafer fabrication processes for the volume production of wafer probe cards. Our proprietary manufacturing processes include wirebonding, photolithography, plating and metallurgical processes, dry and electro-deposition, and complex interconnection system design. The critical steps in our manufacturing process are performed in a Class 100 clean room environment. We also expend considerable resources on the assembly and test of our wafer probe cards and on quality control.

We have deployed state of the art shop floor controls and systems that allow our operators to monitor and optimize manufacturing flows and capacity. We also use statistical process control to further enhance the quality of our production processes.

We depend upon suppliers for some components of our manufacturing process, including ceramic substrates and complex printed circuit boards. Some of these components are supplied by a single vendor. Generally, we rely on purchase orders rather than long-term contracts with our suppliers, which subjects us to risks including price increases and component shortages. We continue to evaluate alternative sources of supply for these components.

We are subject to U.S. federal and state and foreign governmental laws and regulations relating to the protection of the environment. We believe that we comply with all material environmental laws and regulations that apply to us. In May 2003, we received a Notice of Violation from the Bay Area Air Quality Management District regarding our record keeping relating to our usage of wipe cleaning solvent. We introduced corrective action to prevent any continued or recurrent record keeping violation, and we resolved the Notice of Violation with a monetary payment which was not significant. It is possible that in the future, we may receive environmental violation notices, and that final resolution of the violations identified by these notices could harm our operating results. New laws and regulations, stricter enforcement of existing laws and regulations, the discovery of previously unknown contamination at our or others sites or the imposition of new cleanup requirements could have a negative effect on our operating results.

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We maintain a repair and service capability in Livermore, California. Since 2000, we have been providing service and maintenance capabilities in our local service center in Seoul, South Korea. In 2002, we expanded our center in Seoul, South Korea to service a greater part of the Asia Pacific region, and in 2003, we opened a local repair and service center in Dresden, Germany. We plan to expand these capabilities in other geographies to provide faster response time to our customers, maximizing the uptime of their wafer probe cards.

Research and Development

The semiconductor industry is subject to rapid technological change and new product introductions and enhancements. We believe that our continued commitment to research and development and timely introduction of new and enhanced wafer probe test solutions and other technologies related to our MicroSpring interconnect technology are integral to maintaining our competitive position. We are investing considerable time and resources in creating structured processes for undertaking, tracking and completing our development projects, and plan to implement those developments into new product or technology offerings. We expect to continue to allocate significant resources to these efforts and to use automation and information technology to provide additional efficiencies in our research and development activities.

We have historically devoted on average approximately 20% of our revenues to research and development programs. Research and development expenses were $11.3 million for the nine months ended September 27, 2003, $14.6 million for fiscal 2002, $14.6 million for fiscal 2001 and $12.0 million for fiscal 2000.

Our research and development and product engineering activities are directed by individuals with significant expertise and industry experience. As of September 27, 2003, we had 72 employees in research and development, of which 62 worked on the design and development of new interconnect and contact technologies related to our core MicroSpring interconnect technology. Of these employees, 54 are engineers and 29 have PhD or MS degrees. The engineering and science disciplines represented in our research and design and product development include: polymer science, chemistry, chemical engineering, electrochemistry, metallurgy, materials science, electrical engineering, mechanical engineering, electronic packaging and computer science.

Intellectual Property

Our success depends in part upon our ability to maintain and protect our proprietary technology and to conduct our business without infringing the proprietary rights of others. We rely on a combination of patents, trade secret laws, trademarks and contractual restrictions on disclosure to protect our intellectual property rights.

As of September 27, 2003, we had 165 issued patents, of which 90 are United States patents and 75 are foreign patents. The expiration dates of these patents range from 2012 to 2022. Our issued patents cover our core interconnect technology, as well as some of our inventions related to wafer probe cards and testing, wafer-level packaging and test, sockets and assemblies and chips. In addition, as of September 27, 2003, we had 302 patent applications pending worldwide, including 115 United States applications, 169 foreign national or regional stage applications and 18 Patent Cooperation Treaty applications. We do not know whether our current patent applications, or any future patent applications that we may file, will result in a patent being issued with the scope of the claims we seek, or at all, or whether any patents we may receive will be challenged or invalidated. Even if additional patents are issued, our patents might not provide sufficiently broad coverage to protect our proprietary rights or to avoid a third party claim against one or more of our products or technologies.

We have both registered and unregistered trademarks, including FormFactor, MicroSpring, MicroForce, MicroLign, MOST and the FormFactor logo.

We routinely require our employees, customers, suppliers and potential business partners to enter into confidentiality and non-disclosure agreements before we disclose to them any sensitive or proprietary information regarding our products, technology or business plans. We require employees to assign to us proprietary information, inventions and other intellectual property they create, modify or improve.

Legal protections afford only limited protection for our proprietary rights. Despite our efforts to protect our proprietary rights, unauthorized parties may attempt to copy aspects of our products or to obtain and use information that we regard as proprietary. Others might independently develop similar or competing technologies

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or methods or design around our patents. In addition, leading companies in the semiconductor industry have extensive patent portfolios and other intellectual property with respect to semiconductor technology. In the future, we might receive claims that we are infringing intellectual property rights of others or that our patents or other intellectual property rights are invalid. We have received in the past, and may receive in the future, communications from third parties inquiring about our interest in licensing certain of their intellectual property or more generally identifying intellectual property that may be of interest to us. For example, we received such a communication from Microelectronics and Computer Technology Corporation in October 2001, with a follow-up letter in January 2002, inquiring about our interest in acquiring a license to certain of their patents and technology, and from IBM Corporation in February 2002, with a follow-up letter in August 2003, inquiring about our interest and need to acquire a license to IBM patents and technology related to high density integrated probes. Neither the Microelectronics and Computer Technology Corporation communications nor the IBM Corporation communication alleged that we were violating protected proprietary rights or threatened to initiate litigation. We have not engaged in a dialog with Microelectronics and Computer Technology Corporation; we presently anticipate that we will engage in a dialog with IBM Corporation regarding our companies respective intellectual property portfolios. In August 2002, subsequent to our initiating correspondence with Japan Electronic Materials Corporation regarding the scope of our intellectual property rights and the potential applicability of those rights to certain of its wafer probe cards, Japan Electronic Materials Corporation offered that precedent technologies exist as to one of our foreign patents that we had identified, and also referenced a U.S. patent in which it stated we might take interest. For the inquiries we have received to date, we do not believe we infringe any of the identified patents and technology.

We have invested significant time and resources in our technology, and it is possible that we will be required to enforce our intellectual property rights against one or more third parties. We presently believe that it is likely that one or more of our competitors are using methodologies or have implemented structures into certain of their products that are covered by one or more of our intellectual property rights. Litigation may be necessary to defend against claims of infringement or invalidity, to determine the validity and scope of our proprietary rights or those of others, to enforce our intellectual property rights or to protect our trade secrets. If we threaten or initiate litigation, we may be subject to claims by third parties against which we must defend. Intellectual property litigation, whether or not it is resolved in our favor, is expensive and time-consuming and could divert management s attention from running our business. If an infringement claim against us resulted in a ruling adverse to us, we could be required to pay substantial damages, cease the use or sale of infringing products, spend significant resources to develop non-infringing technology, discontinue the use of certain technology or obtain a license to the technology. We cannot predict whether a license agreement would be available, or whether the terms and conditions would be acceptable to us. In addition, many of our customer contracts contain provisions that require us to indemnify our customers for third party intellectual property infringement claims, which would increase the cost to us of an adverse ruling in such a claim. An adverse determination could also prevent us from licensing our technologies and methods to others.

Competition

The wafer probe card market is highly competitive, is comprised of many domestic and foreign companies, and has historically been fragmented with many local suppliers servicing individual customers. Recent consolidation has reduced the number of competitors. Current and potential competitors in the wafer probe card market include AMST Co., Ltd., Cascade Microtech, Inc., ESJ Corporation, Feinmetall GmbH, Japan Electronic Materials Corporation, Kulicke and Soffa Industries, Inc., Micronics Japan Co., Ltd., MicroProbe, Inc., NanoNexus Inc., Phicom Corporation, SCS Hightech, Inc., Tokyo Cathode Laboratory Co., Ltd. and Wentworth Laboratories, Inc., among others. While some of these competitors offer wafer probe cards that address various of the performance limitations presented in wafer probe test, we believe none of them resolves all of the performance issues adequately. In many cases a competitor that solves one or more performance limitations compromises other areas of wafer probe card performance. In addition to the ability to address wafer probe card performance issues, the primary competitive factors in our industry include product quality and reliability, price, total cost of ownership, lead times, the ability to provide prompt and effective customer service, field applications support and timeliness of delivery. We believe that we compete favorably with respect to these factors.

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Some of our competitors are also suppliers of other types of test equipment, or offer both advanced wafer probe cards and needle probe cards, and may have greater financial and other resources than we do. We expect that our competitors will enhance their current wafer probe products and that they may introduce new products that will be competitive with our wafer probe cards. In addition, it is possible that new competitors, including test equipment manufacturers, may offer new technologies that reduce the value of our wafer probe cards.

Additionally, semiconductor manufacturers may implement chip designs that include built-in self-test capabilities or similar functions or methodologies that increase test throughput and eliminate some or all of our current competitive advantages. Our ability to compete favorably is also negatively impacted by low volume orders that do not meet our present minimum volume requirements, by very short cycle time requirements that we cannot meet because of our design or manufacturing processes, by long-standing relationships between our competitors and certain semiconductor manufacturers, and by semiconductor manufacturer test strategies that include low performance semiconductor testers.

Employees

As of September 27, 2003, we had 336 full-time employees, including 72 in research and development, 46 in sales and marketing, 26 in general and administrative functions, and 192 in operations. By region, 301 of our employees were in North America, 20 in Japan, 11 in South Korea and 4 in Europe. None of our employees is covered by a collective bargaining agreement. We believe our relations with our employees are good.

Facilities

Our corporate headquarters and manufacturing facilities are located in six buildings in Livermore, California totaling approximately 73,700 square feet. We lease these facilities under lease agreements expiring between February 2004 and April 2004.

During 2001, we leased additional facilities in Livermore, California totaling approximately 119,000 square feet. The new facility, currently under construction, will be comprised of a campus of three buildings. The lease for this site commenced in stages between November 2001 and June 2002 and will expire in 2011, with options to renew through 2031. We plan to move our operations to our new facility in 2004. We believe that the new facility will be adequate for our needs for the foreseeable future.

We also lease office, repair and service, and/or research and development space totaling approximately 12,000 square feet in Tokyo, Japan; Seoul, South Korea; Munich and Dresden, Germany; and Budapest, Hungary.

Legal Proceedings

From time to time, we may be subject to legal proceedings and claims in the ordinary course of business. As of the date of this prospectus, we are not involved in any material legal proceedings.

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MANAGEMENT

Executive Officers and Directors

Our executive officers and directors, and their ages and positions as of September 27, 2003 are as follows:

Name	Age	Position
Dr. Igor Y. Khandros	49	President, Chief Executive Officer and Director
Benjamin N. Eldridge	42	Senior Vice President of Development and Chief Technical Officer
Yoshikazu Hatsukano	64	Senior Vice President of Asia-Pacific Operations and President of FormFactor K.K.
Peter B. Mathews	41	Senior Vice President of Worldwide Sales
Stuart L. Merkadeau	43	Senior Vice President, General Counsel and Secretary
Jens Meyerhoff	39	Senior Vice President of Operations and Chief Financial Officer
Frans van Wijk	46	Senior Vice President of Marketing and Business Development
Michael M. Ludwig	42	Vice President of Human Resources and Finance, and Controller
Harrold J. Rust	41	Vice President of Operations
Joseph R. Bronson	55	Director
Dr. Thomas J. Campbell	51	Director
Dr. William H. Davidow	68	Chairman of the Board of Directors
G. Carl Everett, Jr.	53	Director
James A. Prestridge	71	Director

Dr. Igor Y. Khandros founded FormFactor in April 1993. Dr. Khandros has served as our President and Chief Executive Officer as well as a Director since April 1993. From 1990 to 1992, Dr. Khandros served as the Vice President of Development of Tessera, Inc., a provider of chip scale packaging technology that he co-founded. From 1986 to 1990, he was employed at the Yorktown Research Center of IBM Corporation as a member of the technical staff and a manager. From 1979 to 1985, Dr. Khandros was employed at ABEX Corporation, a casting foundry and composite parts producer, as a research metallurgist and a manager, and he was an engineer from 1977 to 1978 at the Institute of Casting Research in Kiev, Russia. Dr. Khandros holds a M.S. equivalent degree in metallurgical engineering from Kiev Polytechnic Institute in Kiev, Russia, and a Ph.D. in metallurgy from Stevens Institute of Technology.

Benjamin N. Eldridge has served as our Senior Vice President of Development and Chief Technical Officer since September 2000. Mr. Eldridge also served as our Vice President of Development from June 1997 to September 2000, as our Director of Development from June 1995 to June 1997 and as our Manager of Development Engineering from November 1994 to May 1995. From 1984 to October 1994, he was employed at the TJ Watson Research Center of IBM Corporation, where he held various engineering positions in the Physical Sciences and Computer Science departments. Mr. Eldridge holds a B.S. in electrical engineering from Union College and a M.S. in physics from Rensselaer Polytechnic Institute.

Yoshikazu Hatsukano has served as our Senior Vice President of Asia-Pacific Operations since April 2001, and as the President of FormFactor K.K., our wholly owned subsidiary, since December 1998. From 1961 to October 1998, Mr. Hatsukano was employed by various companies affiliated with Hitachi, Ltd., where he held several management positions including the President of Hitachi Micro Systems, Inc. from 1991 to October 1998 and the Vice General Manager of the Hitachi Semiconductor Design and Development Center from 1990 to 1991. Mr. Hatsukano holds a B.S. in electronics from Kyoto University in Kyoto, Japan.

Peter B. Mathews has served as our Senior Vice President of Worldwide Sales since October 2003. Mr. Mathews served as our Vice President of Worldwide Sales from April 1999 to September 2003, and as our Director, Worldwide Sales and Business Development from March 1997 to April 1999. From May 1992 to March 1997, Mr. Mathews was employed at MicroModule Systems, a manufacturer of multichip modules and interconnect test products, where he most recently held the position of Director of Marketing and Business

Development. From 1989 to May 1992, he served as the U.S. Sales Manager for the Advanced Packaging Systems Division of Raychem Corporation, a component manufacturer for electronic and energy applications that was acquired by Tyco Electronics Ltd. Mr. Mathews holds a B.S. in chemical engineering from Cornell University.

Stuart L. Merkadeau has served as a Senior Vice President since October 2003 and as our General Counsel and Secretary since October 2002. Mr. Merkadeau served as one of our Vice Presidents from October 2002 to September 2003, and as our Vice President of Intellectual Property from July 2000 to October 2002. From 1990 to July 2000, Mr. Merkadeau practiced law as an associate and then a partner with Graham & James LLP, where he specialized in licensing and strategic counseling in intellectual property matters. Mr. Merkadeau is admitted to practice in California and registered to practice before the U.S. Patent and Trademark Office. Mr. Merkadeau holds a B.S. in industrial engineering from Northwestern University and a J.D. from the University of California at Los Angeles.

Jens Meyerhoff has served as our Senior Vice President of Operations since January 2003 and as our Chief Financial Officer since August 2000. He served as a Senior Vice President from August 2000 to January 2003, and as our Secretary from April 2002 to October 2002. From March 1998 to August 2000, Mr. Meyerhoff served as the Chief Financial Officer and the Senior Vice President, Materials at Siliconix Incorporated, a manufacturer of power and analog semiconductor products. From 1991 to February 1998, Mr. Meyerhoff was employed in various corporate controller and financial positions with the North American subsidiaries as well as the German headquarters of Daimler-Benz AG. Mr. Meyerhoff holds a German Wirtschaftsinformatiker degree, which is the equivalent of a finance and information technology degree, from Daimler-Benz s Executive Training program.

Frans van Wijk has served as our Senior Vice President of Marketing and Business Development since November 2002. From September 2000 to June 2001, Mr. van Wijk was employed at ON Semiconductor, a manufacturer of advanced semiconductors, where he served as Vice President and General Manager, Broadband Business Group. From 1988 to September 2000, Mr. van Wijk held various positions at Philips Semiconductors, including Senior Vice President and General Manager, Logic Products Group, and General Manager, International Product Marketing. Mr. van Wijk holds a M.S. in electrical engineering from Delft University of Technology, in Delft, The Netherlands.

Michael M. Ludwig has served as our Vice President of Human Resources and Finance, and Controller since April 2001. From January 1999 to March 2001, Mr. Ludwig was employed at Elo TouchSystems, Inc., a touch screen manufacturing company, where he most recently served as the Vice President, Systems and Services Group. From 1989 to January 1999, Mr. Ludwig was employed by Beckman Coulter, Inc., a medical diagnostics and life sciences equipment manufacturer, and various of its subsidiaries, holding positions including Finance Director, Clinical Chemistry Division; Director, Strategic Planning and Finance; and Controller. Mr. Ludwig holds a B.S. in business administration from California State Polytechnic University at Pomona.

Harrold J. Rust has served as our Vice President of Operations since March 2003. From January 2002 to February 2003, Mr. Rust served as our Vice President of Manufacturing. From April 2001 to December 2001, Mr. Rust served as our Senior Director of Probe Head Manufacturing. From 1984 to April 2001, Mr. Rust held various positions in the Storage Technology Division at IBM Corporation, including Business Operations and Planning Manager, and Manufacturing and Engineering Manager. Mr. Rust holds a B.S. in mechanical engineering from the University of California, Davis and a M.S. in mechanical engineering from Stanford University.

Joseph R. Bronson has served as a Director since April 2002. Mr. Bronson has served as an Executive Vice President of Applied Materials, Inc., a manufacturer of semiconductor wafer fabrication equipment, since December 2000, and a member of the Office of the President and the Chief Financial Officer of Applied Materials since January 1998. Mr. Bronson also served as a Senior Vice President and as the Chief Administrative Officer of Applied Materials from January 1998 to December 2000 and as Group Vice President of Applied Materials from April 1994 to January 1998. Mr. Bronson serves on the Board of Directors of one publicly traded company, Jacobs Engineering Group Inc. Mr. Bronson is a Certified Public Accountant and holds a B.S. in accounting from Fairfield University and a M.B.A. from the University of Connecticut.

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Dr. Thomas J. Campbell has served as a Director since July 2003. Since August 2002, Dr. Campbell has been the Dean of the Haas School of Business at the University of California at Berkeley. Dr. Campbell was a professor at Stanford Law School from 1983 to August 2002. Dr. Campbell served as a U.S. congressman from 1989 to 1993 and from 1995 to January 2001, and as a California state senator from 1993 to 1995. Dr. Campbell holds a B.A., a M.A. and a Ph.D. in economics from the University of Chicago, and a J.D. from Harvard Law School.

Dr. William H. Davidow has served as a Director since April 1995 and as Chairman of the Board of Directors since June 1996. Since 1985, Dr. Davidow has been a general partner of Mohr, Davidow Ventures, a venture capital firm. Dr. Davidow serves as Chairman of the Board of Directors of one publicly traded company, Rambus Inc. Dr. Davidow also serves on the board of directors of one privately held company in addition to FormFactor. Dr. Davidow holds an A.B. and a M.S. in electrical engineering from Dartmouth College, a M.S. in electrical engineering from the California Institute of Technology and a Ph.D. in electrical engineering from Stanford University.

G. Carl Everett, Jr. has served as a Director since June 2001. Mr. Everett founded GCE Ventures, a venture advisement firm, in April 2001. From February 1998 to April 2001, Mr. Everett served as Senior Vice President, Personal Systems Group of Dell Computer Corporation. During 1997, Mr. Everett was on a personal sabbatical. From 1978 to December 1996, Mr. Everett held several management positions with Intel Corporation including, Senior Vice President and General Manager of the Microprocessor Products Group and Senior Vice President and General Manager of the Desktop Products Group. Mr. Everett holds a B.A. in business administration from New Mexico State University.

James A. Prestridge has served as a Director since April 2002. Mr. Prestridge has served as a consultant for Empirix Inc., a provider of test and monitoring solutions for communications applications, since October 2001. From June 2000 to January 2001, Mr. Prestridge served as a consultant to the companies that were amalgamated into Empirix. Mr. Prestridge served as a director of Teradyne Inc., a manufacturer of automated test equipment, from May 1997 until May 2000. Mr. Prestridge was Vice-Chairman of Teradyne from January 1996 until May 2000 and served as Executive Vice President of Teradyne from 1992 until May 2000. Mr. Prestridge currently serves on the board of directors of one privately held company in addition to FormFactor. Mr. Prestridge holds a B.S. in general engineering from the U.S. Naval Academy and a M.B.A. from Harvard University. Mr. Prestridge served as a Captain in the U.S. Marine Corps.

Board of Directors

Our certificate of incorporation and bylaws authorize a board of directors of seven members and presently, our board of directors consists of six directors, who are divided into three classes:

Class I, whose term will expire at the annual meeting of stockholders expected to be held in 2004;

Class II, whose term will expire at the annual meeting of stockholders expected to be held in 2005; and

Class III, whose term will expire at the annual meeting of stockholders expected to be held in 2006.

As a result, only one class of directors will be elected at each annual meeting of stockholders, with the other classes continuing on our board of directors for the remainder of their terms. This classification of our board of directors may make it more difficult for a third party to acquire, or may discourage a third party from acquiring, control of our company. The following individuals serve as our directors:

Dr. Khandros and Dr. Davidow are our Class I directors;

Dr. Campbell and Mr. Everett are our Class II directors; and

Messrs. Bronson and Prestridge are our Class III directors.

Our current directors, other than Dr. Campbell, were elected pursuant to a voting agreement that we entered into with certain holders of our common stock and holders of our preferred stock. Upon the closing of our initial

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public offering, these board designation rights terminated. None of our stockholders has any special rights regarding board representation.

Committees of the Board of Directors

Our board of directors has established three standing committees: the audit committee, the compensation committee and the governing committee.

Audit Committee. The audit committee reviews and evaluates our financial statements, accounting practices and our internal audit and control functions, makes recommendations to our board regarding the selection of our independent auditors and reviews the results and scope of the audit and other services provided by our independent auditors. The members of our audit committee are Messrs. Bronson, Everett and Prestridge.

Compensation Committee. The compensation committee reviews and makes recommendations to our board concerning the compensation and benefits of our officers and directors, administers our stock option and employee benefits plans and reviews general policy relating to compensation and benefits. The members of our compensation committee are Messrs. Bronson and Everett and Dr. Davidow.

Governing Committee. The governing committee considers and makes recommendations to our board of directors regarding candidates to serve as members of our board, develops and makes recommendations to our board of directors regarding corporate governance guidelines, and oversees the evaluation of our board. The members of the governing committee are Messrs. Everett and Prestridge and Dr. Davidow.

Compensation Committee Interlocks and Insider Participation

None of the members of our compensation committee has at any time been one of our officers or employees. None of our executive officers serves or in the past has served as a member of the board of directors or compensation committee of any entity that has one or more of its executive officers serving on our board of directors or our compensation committee.

Director Compensation

Effective fiscal 2003, our independent directors receive annual compensation of $12,500, compensation of $1,000 for each board meeting attended, and compensation of $500 for each board committee meeting attended. Prior to fiscal 2003, our independent directors did not receive cash compensation for their services as directors. Our directors, other than our independent directors, do not receive cash compensation for their services as directors. All of our directors, including our independent members, are reimbursed for their reasonable expenses in attending board and board committee meetings. The following directors were granted options to purchase shares of our common stock in fiscal 2002:

In April 2002, we granted Mr. Bronson an option under the management incentive option plan to purchase 50,000 shares of our common stock at an exercise price of $6.50 per share.

In April 2002, we granted Mr. Prestridge an option under the management incentive option plan to purchase 50,000 shares of our common stock at an exercise price of $6.50 per share.

Each director is eligible to participate in our 2002 equity incentive plan. Under this plan, option grants to directors who are not our employees, or employees of a parent or subsidiary of ours, will be automatic and non-discretionary. Each non-employee director who was a member of our board of directors before our initial public offering and who had not received a prior option grant received an option to purchase 12,500 shares of our common stock effective upon our initial public offering. Each non-employee director who becomes a member of our board of directors on or after our initial public offering will be granted an option to purchase 12,500 shares of our common stock as of the date that director joins the board. When Dr. Campbell became a member of our board of directors in July 2003, we granted him an option under our 2002 equity incentive plan to purchase 12,500 shares of our common stock at an exercise price of $18.72 per share. Immediately after each annual meeting of our stockholders, each non-employee director will automatically be granted an additional option to purchase 12,500 shares of our common stock, as long as the non-employee director is a member of our board on that date and has served continuously as a member of our board for at least 12 months since the last option grant to that non-employee director. If less than 12 months has

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passed, then the number of shares subject to the option granted after the annual meeting will be equal to 12,500 multiplied by a fraction, the numerator of which is the number of days that have elapsed since the last option grant to that director and the denominator of which is 365 days.

Each option will have an exercise price equal to the fair market value of our common stock on the date of grant. The options will have ten-year terms and will terminate three months after the date the director ceases to be a director or consultant or 12 months if the termination is due to death or disability. All options granted to non-employee directors who first became members of our board of directors after our initial public offering will vest over a one-year period at a rate of 1/12th of the total shares granted at the end of each full succeeding month, so long as the non-employee director continuously remains our director or consultant. All succeeding option grants to non-employee directors who were members of our board of directors prior to our initial public offering will vest as to 1/12th of the total shares granted at the end of each full succeeding month from the later of the date of grant or the date when all outstanding stock options and all outstanding shares issued upon exercise of any stock options granted to the non-employee director prior to the grant of such succeeding grant have fully vested. In the event of our dissolution or liquidation or a change in control transaction, options granted to our non-employee directors under the plan will become 100% vested and exercisable in full.

Members of our board of directors, who are employees of FormFactor, or any parent or subsidiary of FormFactor and who own our common stock or hold options to purchase our common stock in an amount less than 5% of our total outstanding shares, are eligible to participate in our 2002 employee stock purchase plan. For additional information, see Employee Benefit Plans and Option Grants 2002 Employee Stock Purchase Plan.

Executive Compensation

The following table presents information regarding the compensation received during fiscal 2002 and 2001 by our chief executive officer and each of our four other most highly compensated executive officers. The compensation table excludes other compensation in the form of perquisites and other personal benefits to a named executive officer where that compensation constituted less than the lesser of $50,000 or 10% of his total annual salary and bonus for such fiscal year.

Name and Principal Position	Year	Annual Compensation		Long-Term Compensation Awards
		Salary	Bonus	Securities Underlying Options
Dr. Igor Y. Khandros	2002	$252,756	$115,800	
President and Chief Executive Officer	2001	228,923	27,943	
Benjamin N. Eldridge	2002	201,387	77,760	94,500
Senior Vice President of Development and Chief Technical Officer	2001	190,769	18,629	52,105
Yoshikazu Hatsukano	2002	237,815(1)	89,115	31,500
Senior Vice President of Asia-Pacific Operations and President of FormFactor K.K.	2001	200,495(2)	20,750(2)	43,770
Jens Meyerhoff	2002	209,849	77,760	142,500
Senior Vice President of Operations and Chief Financial Officer	2001	190,077	15,046	102,485
Peter B. Mathews	2002	251,179(3)		58,500
Senior Vice President of Worldwide Sales	2001	271,565(4)		35,000

(1) The U.S. dollar equivalent of the salary, which is paid to Mr. Hatsukano in Japanese Yen, is calculated using the exchange rate at December 27, 2002 of one U.S. dollar to 119.92 Japanese Yen.

(2) The U.S. dollar equivalent of the salary and bonus, which is paid to Mr. Hatsukano in Japanese Yen, is calculated using the exchange rate at December 28, 2001 of one U.S. dollar to 131.30 Japanese Yen.

(3) Includes $88,099 in sales commissions.

(4) Includes $121,969 in sales commissions.

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Option Grants in Fiscal 2002

The following table presents information regarding grants of stock options during fiscal 2002 to the executive officers named in the executive compensation table above. We granted these options to the named executive officers under our management incentive option plan. All of the options listed on the following table expire ten years from the date of grant and were granted at an exercise price equal to the fair market value of our common stock as determined by our board of directors on the date of grant. The percentage of total options granted to employees in fiscal 2002 is based on options to purchase a total of 1,999,243 shares of our common stock granted in fiscal 2002.

	Individual Grants				Potential Realizable Value At Assumed Annual Rates of Stock Price Appreciation for Option Term	
Name	Number of Securities Underlying Options Granted	% of Total Options Granted to Employees in Fiscal Year	Exercise Price Per Share	Expiration Date	5%	10%
Dr. Igor Y. Khandros		%	$		$	$
Benjamin N. Eldridge	63,000	3.2	6.50	4/17/12	1,663,431	2,891,297
	31,500	1.6	6.50	4/17/12	831,716	1,445,648
Yoshikazu Hatsukano	31,500	1.6	6.50	4/17/12	831,716	1,445,648
Jens Meyerhoff	95,000	4.8	6.50	4/17/12	2,508,349	4,359,892
	47,500	2.4	6.50	4/17/12	1,254,174	2,179,946
Peter B. Mathews	39,000	2.0	6.50	4/17/12	1,029,743	1,789,850
	19,500	1.0	6.50	4/17/12	514,872	894,925

Potential realizable values are calculated by:

multiplying the number of shares of our common stock subject to a given option by $20.20, the closing price per share of our common stock on the Nasdaq National Market on September 26, 2003;

assuming that the aggregate stock value derived from that calculation compounds at the annual 5% or 10% rates shown in the table for the entire ten-year term of the option; and

subtracting from that result the total option exercise price.

The 5% and 10% assumed annual rates of stock price appreciation are required by the rules of the Securities and Exchange Commission and do not represent our estimate or projection of future stock price growth. Actual gains, if any, on stock option exercises will be dependent on the future performance of our common stock.

The options for 63,000 shares of our common stock granted to Mr. Eldridge vest in 12 equal monthly increments beginning on November 21, 2005 and the option for 31,500 shares vests in 12 equal monthly increments beginning on November 21, 2006. The option granted to Mr. Hatsukano vests in 12 equal monthly increments beginning on December 1, 2005. The options for 95,000 shares of our common stock granted to Mr. Meyerhoff vest in 12 equal monthly increments beginning on August 7, 2005 and the option for 47,500 shares vests in 12 equal monthly increments beginning on August 7, 2006. The options for 39,000 shares of our common stock granted to Mr. Mathews vest in 12 equal monthly increments beginning on March 6, 2005 and the option for 19,500 shares vests in 12 equal monthly increments beginning on March 6, 2006. These options provide that the optionholder will receive credit for an additional 12 months of service when calculating the number of shares of our common stock that vest after a change in control of FormFactor where the officer s employment is terminated without cause within 12 months following the change in control transaction.

Aggregate Option Exercises in Fiscal 2002

The following table presents the number of shares of our common stock subject to unexercised options held by the executive officers named in the executive compensation table above at December 28, 2002 and the value of the unexercised options that are in-the-money. This value is calculated based on the difference between $20.20, the closing price per share of our common stock on the Nasdaq National Market on September 26, 2003, and the

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exercise price for the shares underlying the option, multiplied by the number of shares. None of the named executive officers exercised any options to purchase our common stock in fiscal 2002.

Name	Number of Securities Underlying Unexercised Options at December 28, 2002		Value of Unexercised In-The-Money Options at December 28, 2002	
	Exercisable	Unexercisable	Exercisable	Unexercisable
Dr. Igor Y. Khandros			$	$
Benjamin N. Eldridge	316,605		4,754,989	
Yoshikazu Hatsukano	195,270		2,975,199	
Jens Meyerhoff	344,985		4,826,295	
Peter B. Mathews	173,000		2,557,850	

Change of Control and Severance Agreements

In September 2001, our board adopted our key management bonus plan, which provides awards to our chief executive officer, senior vice presidents and vice presidents based upon the target percentage achievement of corporate objectives and personal objectives for these individuals. If a change in control of FormFactor occurs, all bonus awards will be deemed to have been earned at 100% of the bonus target percentage for the current plan year and will be paid to the participants at that time. This plan is administered by the compensation committee of our board of directors. For additional information, see Employee Benefit Plans and Option Grants Key Management Bonus Plan.

Our current stock option agreements for our officers provide that the optionholder will receive credit for an additional 12 months of service when calculating the number of shares of our common stock that vest after a change in control of FormFactor where the officer s employment is terminated without cause within 12 months following the change in control transaction. For additional information, see Employee Benefit Plans and Option Grants.

We have entered into an agreement with Mr. Hatsukano, our Senior Vice President of Asia-Pacific Operations and the President of FormFactor K.K., that provides that if his employment is terminated, he will receive a severance payment equal to one month s base salary for each year of service with us with service for partial years to be prorated. If Mr. Hatsukano s employment is terminated for reasons other than cause, he will receive an additional lump sum payment equal to one month s base salary.

Employee Benefit Plans and Option Grants

Incentive Option Plan

As of September 27, 2003, options to purchase 1,741,763 shares of our common stock were outstanding under our incentive option plan. The options outstanding under the incentive option plan had a weighted average exercise price of $6.01 per share. Our employees who had an annual base salary equal to or greater than $60,000 were eligible to receive awards under the incentive option plan. Since the effectiveness of our 2002 equity incentive plan, we do not grant options under our incentive option plan. However, any outstanding options under our incentive option plan will remain outstanding and subject to our incentive option plan and related stock option agreements until they are exercised or until they terminate or expire by their terms. Outstanding options under our incentive option plan are subject to terms substantially similar to those described below with respect to options granted under our 2002 equity incentive plan.

Management Incentive Option Plan

As of September 27, 2003, options to purchase 1,438,539 shares of our common stock were outstanding under our management incentive option plan. The options outstanding under the management incentive option plan had a weighted average exercise price of $6.32 per share. Our employees, consultants and directors were eligible to receive awards under the management incentive option plan. Since the effectiveness of our 2002 equity incentive plan, we do not grant options under our management incentive option plan. However, any outstanding

options under our management incentive option plan will remain outstanding and subject to our management incentive option plan and related stock option agreements until they are exercised or until they terminate or expire by their terms. Outstanding options under our management incentive option plan are subject to terms substantially similar to those described below with respect to options granted under our 2002 equity incentive plan.

1995 Stock Plan and 1996 Stock Option Plan

As of September 27, 2003, options to purchase 15,000 shares of our common stock were outstanding under our 1995 stock plan. The options outstanding under the 1995 stock plan had a weighted average exercise price of $0.10 per share. Our employees and consultants were eligible to receive awards under the 1995 stock plan. As of September 27, 2003, options to purchase 2,492,462 shares of our common stock were outstanding under our 1996 stock option plan. The options outstanding under the 1996 stock option plan had a weighted average exercise price of $5.55 per share. Our employees, consultants and directors were eligible to receive awards under the 1996 stock option plan. We discontinued granting options under our 1995 stock plan prior to our initial public offering, and, since the effectiveness of our 2002 equity incentive plan, we do not grant options under our 1996 stock option plan. However, any outstanding options under our 1995 stock plan or 1996 stock option plan will remain outstanding and subject to our 1995 stock plan and 1996 stock option plan, as applicable, and related stock option agreements until they are exercised or until they terminate or expire by their terms. Outstanding options under our 1995 stock plan or 1996 stock option plan are subject to terms substantially similar to those described below with respect to options granted under our 2002 equity incentive plan.

2002 Equity Incentive Plan

The 2002 equity incentive plan serves as the successor to our previously existing stock option plans. As of September 27, 2003, options to purchase 1,362,347 shares were outstanding under this plan. The options outstanding under our 2002 equity incentive plan had a weighted average exercise price of $18.17 per share. This plan authorizes the award of options, restricted stock and stock bonuses.

Our 2002 equity incentive plan is administered by the compensation committee of our board of directors, each member of which is an outside director as defined under applicable federal tax laws. Our compensation committee has the authority to interpret this plan and any agreement entered into under the plan, grant awards and make all other determinations for the administration of the plan.

Our 2002 equity incentive plan provides for the grant of both incentive stock options that qualify under Section 422 of the Internal Revenue Code and nonqualified stock options. The incentive stock options may be granted only to our employees or employees of any of our subsidiaries. The nonqualified stock options, and all awards other than incentive stock options, may be granted to our employees, officers, directors, consultants, independent contractors and advisors and those of any of our subsidiaries. However, consultants, independent contractors and advisors are only eligible to receive awards if they render bona fide services not in connection with the offer and sale of securities in a capital-raising transaction. The exercise price of incentive stock options must be at least equal to the fair market value of our common stock on the date of grant. The exercise price of incentive stock options granted to 10% stockholders must be at least equal to 110% of the fair market value of our common stock on the date of grant.

The maximum term of the options granted under our 2002 equity incentive plan is ten years. The awards granted under this plan may not be transferred in any manner other than by will or by the laws of descent and distribution and may be exercised during the lifetime of the optionee only by the optionee. Our compensation committee may allow exceptions to this restriction for awards that are not incentive stock options. Options granted under our 2002 equity incentive plan expire one month after the termination of the optionee s service to us or to a parent or subsidiary of ours for cause, three months if the termination is for reasons other than death, disability or cause, or 12 months if the termination is due to death or disability. In the event of a liquidation, dissolution or change in control transaction, except for options granted to non-employee directors, the options may be assumed or substituted by the successor company. Except for options granted to non-employee directors, options that are not assumed or substituted will expire on the transaction at the time and on the conditions as our

compensation committee will determine. In the event of a change in control transaction in which an optionee, other than a non-employee director, is terminated without cause within 12 months following the change in control, our current stock option agreements provide for 12 months of accelerated vesting of the optionee s shares of our common stock.

As of September 27, 2003, there were 2,210,881 shares of our common stock reserved for issuance under our 2002 equity incentive plan, which includes the shares of our common stock reserved under our incentive option plan, management incentive option plan and 1996 stock option plan that were not issued or subject to outstanding grants on the date of our initial public offering prospectus. The number of shares reserved for issuance under this plan will be increased by:

- the number of shares of our common stock issued under our incentive option plan, management incentive option plan, 1995 option plan or 1996 stock option plan that we repurchase at the original purchase price; and
- the number of shares of our common stock issuable upon exercise of options granted under our incentive option plan, management incentive option plan, 1995 option plan or 1996 stock option plan that expire or become unexercisable at any time after this offering without having been exercised in full.

In addition, under the terms of our 2002 equity incentive plan, the number of shares of our common stock reserved for issuance under the plan will increase automatically on January 1 of each year starting in 2004 by an amount equal to 5% of our total outstanding shares as of the immediately preceding December 31.

Shares available for grant and issuance under our 2002 equity incentive plan include:

- shares of our common stock issuable upon exercise of an option granted under this plan that is terminated or cancelled before the option is exercised;
- shares of our common stock issued upon exercise of any option granted under this plan that we repurchase at the original purchase price;
- shares of our common stock subject to awards granted under this plan that are forfeited or that we repurchase at the original issue price; and
- shares of our common stock subject to stock bonuses granted under this plan that otherwise terminate without shares being issued.

During any calendar year, no person will be eligible to receive more than 1,000,000 shares, or 3,000,000 shares in the case of a new employee, under our 2002 equity incentive plan. Our 2002 equity incentive plan will terminate in 2012, unless it is terminated earlier by our board of directors.

2002 Employee Stock Purchase Plan

The 2002 employee stock purchase plan is designed to enable eligible employees to purchase shares of our common stock at a discount on a periodic basis. Our compensation committee administers the 2002 employee stock purchase plan. Our employees generally are eligible to participate in this plan if they are employed by us, or a subsidiary of ours that we designate, for more than 20 hours per week and more than five months in a calendar year. Our employees are not eligible to participate in our 2002 employee stock purchase plan if they are 5% stockholders or would become 5% stockholders as a result of their participation in the plan. Under the 2002 employee stock purchase plan, eligible employees may acquire shares of our common stock through payroll deductions, or through a single lump sum cash payment in the case of the first offering period. Our eligible employees may select a rate of payroll deduction between 1% and 15% of their cash compensation. For the first offering period, employees were automatically granted an option based on 15% of their cash compensation during the first purchase period. An employee s participation in this plan will end automatically upon termination of employment for any reason. In the event of a change in control transaction, this plan will continue with regard to any offering periods that commenced prior to the closing of the proposed transaction and shares will be

purchased based on the fair market value of the surviving corporation s stock on each purchase date, unless otherwise provided by our compensation committee.

No participant will be able to purchase shares having a fair market value of more than $25,000, determined as of the first day of the applicable offering period, for each calendar year in which the employee participates in the 2002 employee stock purchase plan. Except for the first offering period, each offering period will be for two years and will consist of four six-month purchase periods. The first offering period began on June 12, 2003, the first day on which price quotations were available for our common stock on the Nasdaq National Market. The first purchase period may be more or less than six months long. After that, the offering periods will begin on February 1 and August 1. The purchase price for shares of our common stock purchased under the 2002 employee stock purchase plan will be 85% of the lesser of the fair market value of our common stock on the first day of the applicable offering period or the last day of each purchase period. Our compensation committee has the power to change the starting date of any later offering period, the purchase date of a purchase period and the duration of any offering period or purchase period without stockholder approval if this change is announced before the relevant offering period or purchase period. Our 2002 employee stock purchase plan is intended to qualify as an employee stock purchase plan under Section 423 of the Internal Revenue Code.

We have reserved 1,500,000 shares of our common stock for issuance under the 2002 employee stock purchase plan. The number of shares reserved for issuance under the plan will increase automatically on January 1 of each year, starting in 2004, by an amount equal to 1% of our total outstanding shares as of the immediately preceding December 31. Our board of directors or compensation committee may reduce the amount of the increase in any particular year. The 2002 employee stock purchase plan will terminate in April 2012, unless it is terminated earlier by our board of directors.

Key Management Bonus Plan

In September 2001, our board adopted our key management bonus plan, which provides awards to our chief executive officer, senior vice presidents, vice presidents and other employees based upon the percentage achievement of corporate objectives and personal objectives for these individuals. Bonus target percentages for these awards for each participant level are established for each fiscal year. Corporate objectives are also established for each fiscal year. In fiscal 2003, the corporate objectives are bookings, net sales and operating margin for our company. Personal objectives are determined by the participants in consultation with their immediate supervisors and these objectives are generally critical to the success of the participant in our company and relate to the overall business priorities of FormFactor. For each participant, percentage participation rates are based upon the level of that individual s responsibility and the scope of that individual s work in our organization. In the event of a change of control of FormFactor, all bonus awards will be deemed to have been earned at 100% of the bonus target percentage for the current plan year and will be paid to the participants at that time. This plan is administered by the compensation committee of our board of directors.

Sales Incentive Plan

We have implemented a sales incentive plan that provides incentive commissions to each member of our sales force who is a vice president, director, account manager or regional manager. These commissions are based upon bookings for the region in which the sales member participates and upon management objectives regarding our revenues, backlog and market share. The commissions of each participating member of our sales force are calculated based upon a percentage of that member s base salary with the commission allocated between the bookings targets and the management buy objectives. These incentive commissions are paid on a quarterly basis.

401(k) Plan

We sponsor a defined contribution plan intended to qualify under Section 401 of the Internal Revenue Code, or a 401(k) Plan. Employees are generally eligible to participate in this plan. Participants may make pre-tax contributions to the plan of up to 25% of their eligible earnings, subject to a statutorily prescribed annual limit. Each participant is fully vested in his or her contributions and the investment earnings. We may make matching contributions on a discretionary basis to the 401(k) Plan but had not done so as of September 27, 2003.

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Contributions by us, if any, would generally be deductible by us when made. Contributions are held in trust as required by law. Individual participants may direct the trustee to invest their accounts in authorized investment alternatives.

Indemnification of Directors and Officers and Limitation of Liability

Our certificate of incorporation eliminates the personal liability of a director for monetary damages resulting from any breach of his fiduciary duty as a director, except for liability:

- for any breach of the director s duty of loyalty to us or our stockholders;
- for acts or omissions not in good faith or that involve intentional misconduct or a knowing violation of law;
- for unlawful payments of dividends or unlawful stock repurchases, redemptions or other distributions; or
- for any transaction from which the director derived an improper personal benefit.

Our bylaws provide that:

- we are required to indemnify our directors and officers to the fullest extent permitted by the Delaware General Corporation Law, subject to limited exceptions where indemnification is not permitted by applicable law;
- we are required to advance expenses, as incurred, to our directors and officers in connection with a legal proceeding to the fullest extent permitted by the Delaware General Corporation Law, subject to limited exceptions; and
- the rights conferred in the bylaws are not exclusive.

In addition to the indemnification required in our certificate of incorporation and bylaws, we have entered into indemnification agreements with each of our current directors and executive officers, which may, in some cases, be broader than the indemnification provisions set forth under Delaware law. These agreements provide for the indemnification of our directors and executive officers for all expenses and liabilities incurred in connection with any action or proceeding brought against them by reason of the fact that they are or were our agents. We have also obtained directors and officers insurance to cover our directors, officers and some of our employees for liabilities, including liabilities under the securities laws. We believe that these indemnification provisions and agreements and this insurance are necessary to attract and retain qualified directors and executive officers.

The limitation of liability and indemnification provisions in our certificate of incorporation and bylaws may discourage stockholders from bringing a lawsuit against our directors for breach of their fiduciary duty. They may also reduce the likelihood of derivative litigation against our directors and officers, even though an action, if successful, might benefit us and other stockholders. Furthermore, a stockholder s investment may be adversely affected to the extent that we pay the costs of settlement and damage awards against directors and officers as required by these indemnification provisions. At present, there is no pending litigation or proceeding involving any of our directors, officers or employees regarding which indemnification is sought, and we are not aware of any threatened litigation that may result in claims for indemnification.

Insofar as indemnification for liabilities arising under the Securities Act may be permitted to directors, officers or persons controlling us pursuant to the foregoing provisions, we have been informed that in the opinion of the Securities and Exchange Commission this indemnification is against public policy as expressed in the Securities Act and is therefore unenforceable.

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RELATED PARTY TRANSACTIONS

Since December 27, 1999, we have not been a party to, and we have no plans to be a party to, any transaction or series of similar transactions in which the amount involved exceeded or will exceed $60,000 and in which any current director, executive officer, holder of more than 5% of our common stock or entities affiliated with them had or will have an interest, other than as described under Management and in the transactions described below.

Stock Sales to Insiders

The following table summarizes purchases of our common stock since December 27, 1999 by our executive officers, directors and holders of more than 5% of our common stock.

Purchaser	Shares of Common Stock	Total Purchase Price	Date of Purchase
Dr. Igor Y. Khandros President, Chief Executive Officer and Director	100,000	$600,000	11/14/00
Jens Meyerhoff Senior Vice President of Operations and Chief Financial Officer	100,000	550,000	10/17/00
Stuart L. Merkadeau	42,191	232,051	6/11/03
Senior Vice President, General Counsel and Secretary	36,363	199,997	10/17/00
Dr. William H. Davidow Chairman of the Board of Directors	100,000	650,000	3/13/02
Joseph R. Bronson	10,000	65,000	5/2/02
Director	5,000	32,500	8/19/03

The following table summarizes purchases of our preferred stock since December 27, 1999 by our executive officers, directors and holders of more than 5% of our outstanding stock and entities affiliated with them. We sold 633,130 shares of our Series F preferred stock from September 2000 to November 2000 at $11.00 per share. Each share of our preferred stock converted automatically into one share of our common stock upon the closing of our initial public offering.

Purchaser	Shares of Series F Preferred Stock
Yoshikazu Hatsukano Senior Vice President of Asia-Pacific Operations and President of FormFactor K.K.	5,000
James A. Prestridge Director	348

Registration Rights

We have entered into an investors rights agreement with each of the purchasers of preferred stock listed above. Under this agreement, these and other stockholders and warrant holders are entitled to registration rights with respect to their shares of common stock that were issued upon the automatic conversion of their preferred stock upon the closing of our initial public offering. For additional information, see Description of Capital Stock Registration Rights.

Loans to Executive Officers

In connection with exercises of options to purchase our common stock, the following executive officers and director delivered full recourse promissory notes, each with a six-year term and bearing interest at the annual rate indicated below, compounded semi-annually, on the dates and

in the amounts in the table below. Each note was

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secured by the shares purchased with that note. The following executive officers and director repaid in full the outstanding principal of and unpaid accrued interest on these notes in June 2003.

Borrower	Principal Amount	Interest Rate	Loan Date	Shares Purchased
Dr. Igor Y. Khandros President, Chief Executive Officer and Director	$599,900	5.92%	11/14/00	100,000
Benjamin N. Eldridge	80,000	5.51	2/27/98	100,000
Senior Vice President of Development and	4,500	6.29	8/05/97	45,000
Chief Technical Officer	9,874	5.91	4/08/97	59,840
Jens Meyerhoff Senior Vice President of Operations and Chief Financial Officer	549,900	6.00	10/17/00	100,000
Peter B. Mathews Senior Vice President of Worldwide Sales	8,663	5.91	4/08/97	52,500
Stuart L. Merkadeau Senior Vice President, General Counsel and Secretary	199,960	6.00	10/17/00	36,363

On February 1, 2001, we loaned $150,000 to Mr. Merkadeau, our Senior Vice President, General Counsel and Secretary, under a loan agreement. This loan was evidenced by a full recourse promissory note with an interest rate of 5.01% per year, compounded semiannually. This loan was secured by up to 125,000 shares of our common stock that are issuable to Mr. Merkadeau under a stock option agreement. Mr. Merkadeau repaid in full the outstanding principal of and unpaid accrued interest on this loan in June 2003.

Indemnification Agreements

We have entered into indemnification agreements with each of our current directors and executive officers. These agreements require us to indemnify these individuals to the fullest extent permitted under Delaware law against liabilities that may arise by reason of their service to FormFactor, and to advance expenses incurred as a result of any proceeding against them as to which they could be indemnified. We also intend to enter into indemnification agreements with our future directors and executive officers.

Relationships with Intel Corporation

In connection with the purchase by Intel Corporation of our preferred stock in August 1997, we provided to Intel registration rights with respect to their shares of our common stock issuable upon the automatic conversion of their preferred stock under an investors rights agreement. We have entered into agreements with Intel Corporation under which we sell to them our wafer probe cards and related services. The agreements do not obligate Intel to purchase our products. We sell products based on Intel purchase orders and the terms of the agreements. Under these agreements, we price our products and services to Intel at the lowest price that is charged to any of our other customers for the same products and services. We received $22.5 million in the nine months ended September 27, 2003 and $21.2 million in fiscal 2002 from sales of our wafer probe cards and related installation, training and support services to Intel.

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PRINCIPAL AND SELLING STOCKHOLDERS

The following table presents information regarding the beneficial ownership of our common stock as of September 27, 2003, and as adjusted to reflect the sale of our common stock in this offering, for:

- each person or entity known by us to own beneficially more than 5% of our common stock;
- each of our current directors;
- each of our current executive officers;
- all of our current directors and executive officers as a group; and
- all selling stockholders.

The percentage of beneficial ownership for the following table is based on 34,264,333 shares of our common stock outstanding as of September 27, 2003. The percentage of beneficial ownership after the offering is based on 35,791,828 shares of our common stock outstanding after this offering, assuming no exercise of the underwriters over-allotment option.

Beneficial ownership is determined under the rules and regulations of the Securities and Exchange Commission and does not necessarily indicate beneficial ownership for any other purpose. Under these rules, beneficial ownership includes those shares of common stock over which the stockholder has sole or shared voting or investment power. It also includes shares of common stock that the stockholder has a right to acquire within 60 days of September 27, 2003 through the exercise of any option, warrant or other right, and restricted shares of our common stock, which are subject to a lapsing right of repurchase at their initial purchase price, purchased by some of our officers who exercised immediately exercisable options. The percentage ownership of the outstanding common stock, however, is based on the assumption, expressly required by the rules and regulations of the Securities and Exchange Commission, that only the person or entity whose ownership is being reported has exercised options or warrants into shares of our common stock.

To our knowledge, except under community property laws or as otherwise noted, the persons named in the table have sole voting and sole investment power with respect to all shares beneficially owned. Unless otherwise indicated, each direct