ALTERA CORP
Form 10-K/A
October 24, 2006
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UNITED STATES

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

FORM 10-K/A

(Mark One)

x Annual report pursuant to Section 13 or 15(d) of the Securities

Exchange Act of 1934

For the fiscal year ended December 30, 2005

Or

¨ Transition report pursuant to Section 13 or 15(d) of the Securities

Exchange Act of 1934

For the transition period from _____ to _____

Commission File Number: 0-16617

ALTERA CORPORATION

(Exact Name of Registrant as Specified in its Charter)

Delaware	77-0016691

(State or Other Jurisdiction of Incorporation or Organization)	(I.R.S. Employer Identification No.)
101 Innovation Drive, San Jose, California (Address of Principal Executive Offices)	95134 (Zip Code)

(408) 544-7000

(Registrant s Telephone Number, Including Area Code)

Securities registered pursuant to Section 12(b) of the Act:

None

Securities registered pursuant to Section 12(g) of the Act:

Common Stock, $0.001 par value per share

(Title of Class)

Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. Yes x No ¨

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes ¨ No x

Indicate by check mark whether the registrant: (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes x No ¨

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of registrant s knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K/A or any amendment to this Form 10-K/A. x

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, or a non-accelerated filer (as defined in Rule 12b-2 of the Act).

Large accelerated filer x Accelerated filer ¨ Non-accelerated filer ¨

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Act). Yes ¨ No x

The aggregate market value of the registrant s common stock held by non-affiliates of the registrant was approximately $5,903,001,809 as of July 1, 2005, based upon the closing sale price on the NASDAQ National Market for that date. For purposes of this disclosure, shares of common stock held by persons who hold more than 5% of the outstanding shares of common stock and shares held by executive officers and directors of the registrant have been excluded because such persons may be deemed affiliates. This determination is not necessarily conclusive.

There were 359,297,200 shares of the registrant s common stock, $0.001 par value per share, issued and outstanding as of February 15, 2006.

DOCUMENTS INCORPORATED BY REFERENCE

Items 10, 11, 12, 13, and 14 of Part III incorporate information by reference from the Proxy Statement for the Annual Meeting of Stockholders held on May 9, 2006 and filed with the Securities and Exchange Commission on April 3, 2006 except as to the information updated as a result of this restatement (see Item 11 Executive Compensation).

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EXPLANATORY NOTE

Restatement of Consolidated Financial Statements

We are amending our annual report on Form 10-K for the fiscal year ended December 30, 2005 (the Original Filing) to reflect the restatement of our consolidated financial statements and the related disclosures, for the fiscal years ended 2005, 2004 and 2003 and for each of the quarters in fiscal year 2004. The effects of this restatement on the fiscal year ended December 30, 2005 were negligible and therefore we did not restate any fiscal 2005 consolidated financial statements, except to reflect the cumulative restatement adjustments made to the consolidated balance sheet as of December 30, 2005 as well as a negligible change to fully diluted shares outstanding. We also are restating the pro forma disclosures for stock-based compensation expense required under Statement of Financial Accounting Standards No. 123, Accounting for Stock-Based Compensation, (SFAS 123) included in Note 2 to the consolidated financial statements. This Form 10-K/A also reflects the restatement of Selected Consolidated Financial Data for the fiscal years ended 2005, 2004, 2003, 2002, and 2001 in Item 6 of this Form 10-K/A. The Original Filing was filed with the Securities and Exchange Commission (SEC) on March 14, 2006.

Our decision to restate our consolidated financial statements was based on facts obtained by management and the results of an independent investigation into our stock option accounting that was conducted under the direction of a special committee of the board of directors. On May 3, 2006, our Chief Executive Officer and General Counsel, on their own initiative, commenced a review of the company s historical stock option practices. On May 6, 2006, the board of directors formed a special committee composed solely of independent directors and tasked the committee with the responsibility to conduct a review of the company s historical stock option practices and related accounting. The special committee, with the assistance of its independent legal counsel and forensic accountants, undertook a comprehensive internal review of the facts giving rise to the restatement described below. The investigation included an extensive review of our accounting policies, accounting records, supporting documentation, and e-mail communications, as well as interviews with numerous current and former employees and current and former members of our board of directors.

On June 21, 2006, we announced that our audit committee, after consultation with management and the special committee, determined that our prior consolidated financial statements and any related reports of our independent registered public accounting firm should no longer be relied upon and would be restated. Although we do not believe that the effects of the restatement are material to the results of operations for our fiscal years ended 2005, 2004, or 2003, we are restating prior financial statements because the alternative method of correcting the error, which is to record the cumulative impact of the corrections in the quarter ended March 31, 2006, would result in a material charge to that period and such a charge would likely have a material impact on our fiscal year ended December 29, 2006.

Management concurs with the special committee s conclusion that from December 1996 through February 2001 there were seven occasions on which the recorded grant dates for certain employee stock option grants differed from the actual grant dates. None of these employee stock option grants was made to our current CEO. The price of Altera s stock on the recorded grant dates was lower than the price on the actual grant date thus permitting recipients to exercise these options at a lower strike price. On six occasions, the grants had intrinsic value at the time of grant; that is, they were issued in-the-money . On the seventh occasion, the grants were repriced shortly after the grant date and did not result in a material charge. Under these circumstances, we should have amortized the in-the-money portion of the options over their vesting periods in our previously issued financial statements. To correct this error, we are recording $17.8 million of additional pre-tax, non-cash stock-based compensation expense in the restatement for the periods 1996 to 2004.

The special committee also concurred with management s conclusion that from 1996 to 2002, certain employees stock option agreements were modified in connection with the termination of their employment. Generally these modifications were made in the context of separation agreements that permitted additional vesting and/or additional time to exercise options after the employee had ceased performing services and beyond the periods originally specified in the stock option grant agreements. At the time these agreements were entered into, the Company, did not have sufficient controls in place to ensure that the accounting consequences of these transactions were properly identified, accounted for and reported in the proper period.

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As a result, we should have recorded additional stock-based compensation expense related to the modifications in our previously issued financial statements. To correct this error, we are recording $24.3 million of additional pre-tax, non-cash stock-based compensation expense in the restatement for the periods 1996 to 2002. The majority of this expense relates to only a limited number of modifications that provided an extension of the exercise period for options that were already vested at the time of the modification and approximately 75 percent of this additional expense is attributable to years 1996 and 1997. For more information regarding the investigation and findings relating to stock option practices and the restatement, please refer to Item 7, Management s Discussion and Analysis of Financial Condition and Results Restatement of Consolidated Financial Statements and Related Proceedings , and Note 3 Restatement of Previously Issued Consolidated Financial Statements in Item 8. For more information regarding the investigation and findings relating to stock option practices and the restatement and our remedial measures, see Item 9A, Controls and Procedures.

We have not amended any of our other previously filed annual reports on Form 10-K for the periods affected by the restatement or adjustments other than this amended Annual Report on Form 10-K/A. For this reason, the consolidated financial statements and related financial information contained in such previously filed reports should no longer be relied upon. Except for the sections of this Form 10-K/A listed below, all of the information in this amended Annual Report on Form 10-K/A is as of December 30, 2005 and does not reflect events occurring after the Original Filing. In addition, in accordance with applicable SEC rules, this amended Annual Report on Form 10-K/A includes updated certifications from our Chief Executive Officer (CEO) and acting Chief Financial Officer as Exhibits 31.1, 31.2, 32.1 and 32.2.

For the convenience of the reader, this amended Annual Report on Form 10-K/A sets forth the Original Filing in its entirety, as modified and superseded where necessary to reflect the restatement. The following items have been amended principally as a result of, and to reflect, the restatement, and no other information in the Original Filing is amended hereby as a result of the restatement:

Part I Item 1A: Risk Factors;

Part I Item 3: Legal Proceedings;

Part II Item 6: Selected Consolidated Financial Data;

Part II Item 7: Management s Discussion and Analysis of Financial Condition and Results of Operations;

Part II Item 8: Financial Statements and Supplementary Data;

Part II Item 9A: Controls and Procedures;

Part III Item 11: Executive Compensation; and

Part IV Item 15: Exhibits and Financial Statement Schedules.

FORWARD-LOOKING STATEMENTS

This report and certain information incorporated herein by reference contains forward-looking statements, which are provided under the safe harbor protection of the Private Securities Litigation Reform Act of 1995. Forward-looking statements are generally written in the future tense and/or are preceded by words such as will, may, should, could, expect, suggest, believe, anticipate, intend, plan, or other similar words. Forward-looking statements include statements regarding:

our gross margins and factors that affect gross margins (see Item 7: Management s Discussion and Analysis of Financial Condition and Results of Operations Executive Overview and Item 7: Management s Discussion and Analysis of Financial Condition and Results of Operations Gross Margin);

the commercial success of our new products (see Item 1: Business and Item 7: Management s Discussion and Analysis of Financial Condition and Results of Operations Executive Overview);

our research and development expenditures and efforts (see Item 7: Management s Discussion and Analysis of Financial Condition and Results of Operations Research and Development Expenses);

our capital expenditures (see Item 7: Management s Discussion and Analysis of Financial Condition and Results of Operations Financial Condition, Liquidity, and Capital Resources);

the growth prospects of the semiconductor industry and PLD market, including the FPGA and CPLD product sub-segments (see Item 1: Business Strategy and Competition and Item 7: Management s Discussion and Analysis of Financial Condition and Results of Operations Executive Overview);

trends in our future sales, including our opportunities for growth by displacing ASICs, ASSPs and other fixed chip alternatives and our belief that maintaining or increasing market share in the FPGA product sub-segment is important to our success (see Item 1: Business Strategy and Competition and Item 7: Management s Discussion and Analysis of Financial Condition and Results of Operations Executive Overview);

the impact of new accounting pronouncements, including Statement of Financial Accounting Standards No. 123 (revised 2004), Share-Based Payment, on our expenses (see Item 7: Management s Discussion and Analysis of Financial Condition and Results of Operations);

potential Section 409A remedial actions and additional expenses associated with our stock option investigation, litigation defense and financial restatement (see Item 7: Management s Discussion and Analysis of Financial Condition and Results of Operations Restatement of Consolidated Financial Statements and Related Proceedings Restatement of Consolidated Financials);

changes to improve our controls relating to the process of granting stock option awards (see Item 9A: Controls and Procedures Management s Consideration of the Restatement Stock Option Grant Measurement Date Errors); and

efforts to improve internal control over financial reporting and progress towards remediation of the company s material weakness and mitigation of control deficiencies (see Item 9A: Controls and Procedures Changes in Internal Control Over Financial Reporting).

Forward-looking statements are not guarantees of future performance and involve risks and uncertainties. The forward-looking statements contained in this report are based on information currently available to us and expectations and assumptions that we deem reasonable at the time the statements were made. We do not undertake any obligation to update any forward-looking statements in this report or in any of our other communications, except as required by law. All such forward-looking statements should be read as of the time the statements were made in the Original Filing, unless modified and superseded in this report, and with the recognition that these forward-looking statements may not be complete or accurate at a later date.

Many factors may cause actual results to differ materially from those expressed or implied by the forward-looking statements contained in this report. These factors include, but are not limited to, those risks set forth in Item 1A: Risk Factors.

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PART I

ITEM 1. BUSINESS.

Founded in 1983, Altera Corporation designs, manufactures, and markets: (1) programmable logic devices, or PLDs; (2) our HardCopy® structured application-specific integrated circuit, or ASIC, devices; (3) pre-defined design building blocks known as intellectual property, or IP cores; and (4) associated development tools. Our headquarters facility is located at 101 Innovation Drive, San Jose, California 95134, and our web-site is www.altera.com. Our common stock trades on the NASDAQ National Market under the symbol ALTR.

Our PLDs, which consist of field-programmable gate arrays, or FPGAs, and complex programmable logic devices, or CPLDs, are semiconductor integrated circuits that are manufactured as standard chips that our customers program to perform desired logic functions within their electronic systems. Our HardCopy devices enable our customers to transition from a high-density FPGA to a low-cost non-programmable implementation of their designs for volume production. Our customers can license IP cores from us for implementation of standard functions in their PLD designs. Customers develop, compile, and verify their PLD designs, and then program their designs into our PLDs using our proprietary development software, which operates on personal computers and engineering workstations.

We were one of the first suppliers of complementary metal oxide semiconductor, or CMOS, PLDs and are currently a global leader in this market. Today, we offer a broad range of PLDs that offer unique features as well as differing densities and performance specifications. Our products serve a wide range of customers within the communications, computer and storage, consumer, and industrial market segments. An overview of typical PLD applications within these markets is shown in the table below.

MARKET SEGMENT	MARKET SUB-SEGMENT	APPLICATION/PRODUCT
COMMUNICATIONS	NETWORKING	Routers
		Switches
	WIRELINE	Access Systems
		Metropolitan Area Networks
		Optical Networks
	WIRELESS	Cellular Base Stations
		Wireless Local Area Networks
COMPUTER AND STORAGE	COMPUTER	Mainframes
		Servers

	Office Automation	Copiers
		Multi-Function Peripherals
		Printers
	Storage	Redundant Array of Inexpensive Disks (RAID) Systems
		Storage Area Networks
Consumer	Broadcast	Studio Editing
		Satellite Equipment
		Broadcasting Equipment
	Entertainment	Audio/Video Systems
		Video Displays, Cable Set Top Boxes
Industrial	Automotive	Car Entertainment Systems
		Navigation Systems
	Instrumentation	Manufacturing Systems
		Medical Diagnostic Systems
		Test Equipment
	Military	Guidance and Control
		Radar Systems
		Secure Communications
	Security /Energy Management	Automatic Teller Machines (ATMs)
		Card Readers
		Energy Management Systems

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Digital Logic Overview

Three principal types of digital integrated circuits are used in most electronic systems: (1) processors, (2) memory, and (3) logic.

Processors, which include microprocessors, microcontrollers, and digital signal processors, are typically used for control, central computing tasks, and signal processing;

Memory is used to store programming instructions and data; and

Logic is typically used to manage the interchange and manipulation of digital signals within a system.

While system designers employ a relatively small number of standard architectures to meet their processor and memory needs, they require a wide variety of logic circuits to differentiate their end products.

The majority of the digital logic market is made up of three product sub-segments: (1) ASICs; (2) application-specific standard products, or ASSPs; and (3) PLDs. In a broad sense, all of these products are competitive with each other as they generally may be used in the same types of applications in electronic systems. However, differences in cost, performance, density, flexibility, ease-of-use, and time-to-market dictate the extent to which they may be directly competitive for particular applications. The table below summarizes key characteristics of ASIC, ASSP, and PLD products from the perspective of the end customer.

	ASIC	**ASSP**	**PLD**
Customizable	Yes, by chip fabrication facility	No	Yes, by end user
Erasability/ Re-programmability	No	No	Yes
Relative Time-to-Market	Slow	Immediate	Fast
Relative Unit Cost	Low	Moderate	Moderate to High
Customer s Development Cost	High	Low	Moderate

ASICs, also referred to as standard cells, are defined by the end customer and customized during manufacturing at the chip fabrication facility. As a result, a given ASIC has a fixed function for use by a single customer in a single application. ASSPs are defined by the ASSP supplier and sold as standard devices that cannot be customized by the end user. Rather than being built for a single customer as in the case of an ASIC, an ASSP is built for a specific type of application and is typically targeted and sold to a limited number of customers. For simplicity, an ASSP may be viewed as an ASIC developed for more than one customer. In contrast to the fixed nature of both ASICs and ASSPs, PLDs are customized by the end customer and hence can be used in a wide range of applications. As a result, a given PLD is typically sold to hundreds or thousands of customers.

The inherent flexibility of PLDs provides significant advantages over ASICs, including design change simplicity, shorter design cycles, and lower development cost. In contrast to ASIC users, PLD users program their design directly into the PLD and can have custom chips that are fully functioning and verified at the time the design is completed, thereby bypassing the lengthy and complex cycles involved in the verification and fabrication of ASICs. As a result of user programmability, PLD customers may experiment with and revise their designs in a relatively short amount of time and with minimum development cost. The ease-of- use and time-to-market advantages of PLDs are complemented by the added benefit of field upgradeability, which generally enables PLD users to modify the PLD design after the electronic system has been shipped.

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Due to their programmability, however, PLDs generally have a larger die size and associated higher per-unit cost when compared to ASICs. While the customized manufacturing of ASICs can result in more optimized chip performance and lower per-unit cost than PLDs, ASICs require higher up-front costs and longer manufacturing lead times.

Historically, due to their lower per-unit costs, ASICs have been viewed as more cost effective than PLDs for large-volume, low-cost applications such as consumer electronics. Consequently, the unit volume of a PLD implementation is typically lower than that for an ASIC implementation. Additionally, some customers may choose to prototype with PLDs for initial engineering development and then re-design to an ASIC in volume production for lower per-unit cost. While such re-designs have always been an aspect of the PLD business, we believe that the following factors are driving electronic systems manufacturers to use PLDs for their systems entire life cycle: (1) the continual reduction in the price premium of programmable logic; (2) the ever-shortening product life cycle of many electronic systems; and (3) the use of more advanced chip manufacturing technology, which heightens the failure risk of ASICs and the up-front costs of design, verification and mask development, known as non-recurring engineering costs, or NREs.

ASSPs have been used in applications where specific fixed functions are needed and where little differentiation is required, such as in implementing certain electronic industry standards. However, the fixed functionality of ASSPs limits the range of applications they can address. In contrast to ASSPs, the flexibility found in PLDs allows users to define circuitry to suit their value-added and differentiated system architecture, rather than restrict their system architecture based upon the ASSP manufacturer s device specification. Furthermore, the emergence of IP design blocks in PLDs has allowed the implementation of standardized functions otherwise performed by ASSPs.

We believe that the adoption of more advanced chip manufacturing technology, which is increasing the total cost of chip development, is reducing the cost advantage of ASICs and ASSPs. The cost and time for us to develop a PLD is comparable to the cost and time for others to develop an ASIC or ASSP. Since each of our PLDs is sold to hundreds or thousands of customers, we generally spread development costs and generate revenue across a wide customer base. In contrast, ASIC and ASSP suppliers build fixed, custom chips for a single customer or for a single application. Because it is increasingly difficult for ASIC and ASSP suppliers to identify opportunities that generate enough revenue to compensate for the high development costs, we believe that ASIC suppliers are imposing ever-higher up-front costs and minimum order quantities on customers, and ASSP manufacturers may be developing fewer products.

Strategy and Competition

We believe that the increasing cost associated with the use of advanced chip manufacturing technology is driving the development and use of standard, programmable digital integrated circuits. As in microprocessors and memory, PLDs provide the flexibility for the end user to change and define circuits without incurring the cost, risk and delays of custom chip fabrication. Consequently, we believe that customers will increasingly use PLDs for both prototyping and production rather than ASICs or ASSPs, despite the higher per-unit cost of PLDs.

In order to capture a larger percentage share of the semiconductors purchased by our customers, we are focused on providing the most advanced programmable solutions. To accomplish this goal, we strive to offer our customers:

- PLDs with the speed, density, functionality, and package types to meet their specific needs;

PLDs optimized for low-cost and high-volume applications;

HardCopy devices that enable our customers to easily move from our largest PLDs to a low-cost structured ASIC implementation of their designs;

Optimized, pre-verified system-level IP cores to speed their design process;

State-of-the-art development tools that offer low cost and ease-of-use and compatibility with other industry-standard electronic design automation, or EDA, tools; and

A complete customer support system.

We believe that the greatest opportunity for our growth is displacing ASICs and ASSPs. We compete with other PLD vendors to realize this opportunity and for market share within the PLD market. The programmable logic market is highly concentrated with two vendors accounting for a majority of the total market: ourselves and Xilinx, Inc. Using publicly available data and

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information obtained from Gartner Dataquest, we estimate that the smaller vendors, including Lattice Semiconductor Corporation and Actel Corporation, together comprise approximately 16% of the PLD market. Within the PLD market, sales of FPGAs and CPLDs constitute the majority of revenues. CPLDs and FPGAs are often viewed as two distinct sub-segments of the PLD market and, due to product differences, generally do not compete directly for the same customer designs. Altera was an early entrant in the CPLD sub-segment and, based on our estimates, has held over 40% market share for more than five years. The FPGA sub-segment has outgrown the CPLD sub-segment. FPGAs now comprise approximately 75% of total PLD sales, and it is generally accepted by participants and observers of the industry that the FPGA sub-segment will continue to be the fastest growing sub-segment of the PLD market. Based on our estimates, we believe that in 2005 we had a 32% share in the FPGA sub-segment, up from 30% in 2004 and 29% in 2003, and that maintaining or increasing market share in this sub-segment is important to our long-term growth.

Competition among vendors is most intense in the design-win phase of the customer s design. The design-win phase refers to the customer s selection of a particular vendor s product for use in the customer s electronic system. Because each vendor s product offering is proprietary, the cost to switch PLD devices after a system has been designed and prototyped is very high. Therefore, customers rarely switch PLD vendors after this initial selection for a particular design. From the time a design-win is secured it can be as long as two years, and sometimes longer, before the customer starts volume, or production, purchases of our devices. Typically, the customer selects the PLD vendor relatively early in the customer s design program. It typically takes several years from that point before the customer has completed its entire system design, built prototypes, sampled the marketplace for customer acceptance, made any modifications, and established volume manufacturing capacity. Thus, movements in PLD market share often occur some time after the change in relative competitiveness that gave rise to the market share shift. Because of this time lag, market share is a lagging indicator of relative competitive strength. Because it is extremely difficult to forecast the degree of success or timing of a customer s program, and because the end markets are so fragmented (we have over 14,000 PLD customers), it is difficult even for PLD vendors to gauge their competitive strength in securing design wins as of a particular point in time.

Principal competitive factors in the programmable logic sub-segment include:

- Technical innovation;
- Device performance and features;
- Capability of software development tools and IP cores;
- Pricing and availability;
- Quality and reliability;
- Technical service and customer support;
- Manufacturing and operational competence; and
- Customer familiarity with existing vendors and entrenched products.

We believe that we compete favorably with respect to these factors and that our proprietary device architecture and our installed base of software development systems may provide some competitive advantage. We have been able to introduce new product families that, as compared to their predecessors, provide greater functionality at a lower price for any given density because of unique architectural innovation and advanced technologies.

We also believe that in certain circumstances these new product families compete favorably against ASICs and ASSPs, as well as against other types of chips such as microcontrollers, microprocessors, and digital signal processors. Some of the functionality offered by these other types of chips can be implemented in PLDs using pre-built and pre-verified IP cores. An IP core is typically offered in either a hard or soft form. A hard IP core is embedded into the actual circuitry of our chips. A soft IP core is a licensed design file that our customers incorporate into their design and program onto the PLD. By incorporating more functionality and logic capacity on a programmable chip while providing the necessary design tools and IP cores to design a reliable system, we believe we can enhance the advantages of PLDs over competing solutions.

As is true of the semiconductor industry as a whole, the digital logic segment and the PLD sub-segment are intensely competitive and are characterized by rapid technological change, rapid rates of product obsolescence, and price erosion. All of these factors may adversely affect our future operating results. For a discussion of risk factors associated with our strategy and competition, see Item 1A: Risk Factors *Our failure to compete successfully in the highly competitive semiconductor industry would adversely affect our financial results and business prospects* and *Our failure to define, develop, and manufacture technologically-advanced products would adversely affect the success and growth of our company.*

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Products

Our products consist primarily of devices, IP cores, and proprietary development tools. A brief overview of these products follows.

Devices

Our devices fall into the following four categories: (1) FPGAs, (2) CPLDs, (3) low-cost HardCopy structured ASIC devices, and (4) configuration devices that store the programming code for our FPGAs. These devices span multiple architectures and device families, with numerous product options. Each device family offers unique functional benefits and differing density and performance specifications. Sales of FPGAs accounted for 70% of our total sales in 2005, 68% in 2004 and 65% in 2003. Sales of CPLDs accounted for 20% of our total sales in 2005, 23% in 2004 and 27% in 2003. Sales of our other products accounted for 10% of our total sales in 2005 and less than 10% of our total sales in 2004 and 2003. Some of our latest device families, which are typically designed into new end equipment, are summarized and described below. Certain of our more mature device families, which are not now typically designed into new end equipment but may still comprise significant portions of our total revenue, have been omitted from the descriptions below.

Stratix® and Stratix II High-End, System-Level FPGAs

Our Stratix product families are built using the most advanced CMOS process technology and address a broad range of applications in communications, computing and storage, consumer, and industrial markets. Architectural innovations within Stratix FPGAs help provide industry-leading logic density and performance, while offering high speed and flexible embedded system functionality such as memory and digital signal processing (DSP) blocks. Additionally, our Stratix GX and Stratix II GX FPGA devices offer advanced transceiver capabilities for applications that require reliable, multi-gigabit data transfer rates.

Cyclone and Cyclone II Low-Cost, High-Volume FPGAs

Our Cyclone product families are built using advanced CMOS process technology and bring programmable flexibility to cost-sensitive applications across a vast array of end markets within communications, computing and storage, consumer, and industrial. Architectural innovation allows Cyclone devices to combine a low-cost structure with abundant device resources making them ideal for high-volume applications across all our served markets in areas such as digital set-top boxes, DVD player/recorder systems, automotive telematics, and flat panel televisions.

MAX® and MAX II CPLDs

Our MAX CPLD product families are instant-on, non-volatile devices that address a wide range of high-speed glue logic functions found in a broad range of electronics equipment in the communications, computing and storage, consumer, and industrial markets. Glue logic enables the interaction of multiple subsystem components. Our current generation MAX II devices are based on a newly

developed and revolutionary architecture that reduces costs by up to 50 percent or more, consumes 90 percent less power, and increases performance by as much as 50 percent over the previous generation MAX family.

HardCopy and HardCopy II Structured ASIC Devices

Our HardCopy and HardCopy II (HardCopy) products offer customers a migration path from the highest density FPGA families to a low-cost structured ASIC device for high-volume production applications. In contrast to traditional ASICs, in which every mask layer is custom and unique to the customer s design, structured ASICs share a common set of base layers and the customer s design is implemented in the device by customizing only the last few mask layers. For a given process technology, structured ASIC devices deliver nearly the performance of comparable ASICs, but with reduced development costs and shorter production lead-times.

HardCopy device base arrays are developed from equivalent FPGAs by removing the configuration circuitry, programmable routing, and programmability for logic and memory. This scheme reduces the die size while maintaining compatibility with the FPGA architecture, providing seamless migration of the customer design to a HardCopy device. As a result, HardCopy devices extend the flexibility and time-to-market advantages of high-density FPGAs, which are used typically for prototyping, to high-volume, more cost-sensitive applications traditionally served by fixed ASICs.

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INTELLECTUAL PROPERTY CORES

IP cores are pre-verified building blocks that implement standard system-level functions that customers incorporate in their PLD design by using our proprietary development software. Soft IP cores available for use in our devices consist of our Nios® and Nios II soft core embedded processors and our portfolio of MegaCore® functions, which we license to our customers, and our Altera Megafunction Partners Program, or AMPP℠, cores, which are pre-verified by us and licensed to our customers by third parties.

The Nios and Nios II embedded processors utilize a reduced instruction set computing, or RISC, architecture and are a cost-competitive and flexible alternative to discrete microcontroller solutions. The Nios embedded processors can be efficiently implemented in all of our newer FPGA devices. The Nios II soft core embedded processor provides up to a 300% improvement in price/performance when compared to the original Nios embedded processor and competes favorably with many discrete microcontrollers.

With IP cores, system designers can focus more time and energy on improving and differentiating the unique aspects of their system design, rather than spending time designing common off-the-shelf functions. IP cores are essential to providing our customers solutions that enable higher levels of integration and faster time-to-market. Today, we offer a broad range of soft IP cores for various system blocks for DSP algorithms, bus interfaces, memory controllers, telecommunications, data communications, microprocessors, and peripherals. Prior to licensing a soft IP core, customers may download an encrypted soft IP core from our web-site and verify that it works in their own system design. While licensing soft IP cores represents a small portion of our total revenues, we believe a broad product offering in this area is necessary to compete with ASIC and ASSP suppliers as well as other PLD suppliers.

DEVELOPMENT TOOLS

Our proprietary development tools, consisting primarily of the Quartus® II software, enable our customers to successfully complete all necessary PLD design steps. Our tools enhance engineering productivity by facilitating design entry, design compilation, design verification, and device programming during the initial design and subsequent design revisions.

Our development tools can be used on a variety of computing platforms and have built-in interfaces with other engineering design software, thus making it possible for customers to utilize their existing design environment. Our Quartus II software development tools run under the Microsoft Windows, UNIX (including Solaris and HP-UX), and Linux operating environments. Our development tools also provide interfaces to many industry-standard EDA tools, including those offered by Cadence Design Systems, Inc., Mentor Graphics Corporation, Synopsys, Inc., and Synplicity, Inc.

Like soft IP cores, our development tools generate less than 10% of our total revenues, but are a critical and necessary element of our product portfolio because they are used to program our devices and can drive our success in competing for design wins against ASIC and ASSP suppliers as well as other PLD suppliers.

Research and Development

Our research and development activities have focused primarily on PLDs and on associated IP cores, development software, and hardware. We have developed these related products in parallel to provide comprehensive design support to customers. As a result of our research and development efforts, we have introduced during the past three years a number of new families, including the Stratix II, Stratix II GX, Cyclone II, MAX II, and HardCopy II device families, as well as major enhancements to our IP core offering and the Quartus II development platform.

Our research and development expenditures were $209.8 million in 2005, $181.9 million in 2004, as restated, and $181.3 million in 2003, as restated, which includes stock-based compensation expense as a result of the restatement disclosed in Note 3 Restatement of Previously Issued Financial Statements to our Consolidated Financial Statements. We expense as incurred all research and development costs that have no alternative future use. We intend to continue to spend substantial amounts on research and development in order to continue to develop and achieve market acceptance of our new products. For a discussion of risk factors associated with our research and development efforts, see Item 1A: Risk Factors *Our failure to define, develop, and manufacture technologically-advanced products would adversely affect the success and growth of our company*.

Patents, Trademarks, and Licenses

We generally rely on intellectual property law, including patent, copyright, trademark, and trade secret laws, to establish and maintain our proprietary rights in products and technology. We have increased investment in intellectual property protection in the

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last several years and, as of December 30, 2005, we owned more than 1,100 United States and 180 foreign patents. We also have more than 900 patent applications currently pending. Also, we have used, registered, and applied to register certain trademarks and service marks to distinguish our products, technologies, and services from those of our competitors in the United States and foreign countries. In addition, we file registrations in the United States under the Semiconductor Chip Protection Act to protect our chip designs.

We have entered into technology licensing agreements that give us rights to design, manufacture, and sell products using certain intellectual property owned by others. In July 2001, we entered into a settlement agreement with Xilinx under which we settled all pending patent litigation. As part of the settlement agreement, we entered into a royalty-free patent cross license agreement with Xilinx, including a prohibition of further patent litigation between the two companies through July 2006. In connection with the settlement agreement, we paid Xilinx a one-time payment of $20.0 million. Similarly, in July 2001, we entered into a settlement agreement with Lattice under which we settled all pending patent litigation. As part of the settlement agreement, we entered into a royalty-free patent cross license agreement with Lattice, including a multi-year prohibition of further patent litigation between the two companies. No payments were made by Altera or Lattice as part of the settlement.

When necessary, we seek to enforce our intellectual property rights. For example, in 1999, we brought an action against Clear Logic, Inc. for infringement of our mask work registration rights and for interfering with our license agreements with our customers. A jury in the United States District Court for the Northern District of California decided in our favor on both issues in October 2002, and the jury verdict was affirmed on appeal by the Ninth Circuit Court of Appeals in September 2005. Although we believe that protection afforded by our intellectual property rights has value, the rapidly changing technology in the semiconductor industry makes our future success dependent primarily on the innovative skills, technological expertise, and management abilities of our employees rather than on our patent, trademark, or other proprietary rights. For a discussion of risk factors associated with our patents, trademarks, and licenses, see Item 1A: Risk Factors *The failure of our intellectual property rights to provide meaningful protection from our competitors could harm our competitive position* and *Intellectual property infringement claims could adversely affect our ability to manufacture and market our products.*

Marketing and Sales

We market our products worldwide through a network of distributors, independent sales representatives, and direct sales personnel. From time to time, we may add or remove independent sales representatives or distributors from our selling organization as we deem appropriate.

Altera Distributors

We engage distributors in all major geographic markets that we serve. These distributors are franchised by component manufacturers to sell a wide variety of products to many customers, and they may sell competing products or solutions. We have contracts with our distributors, which can be terminated by either party in a relatively short period of time. The main roles of our independent distributors are to provide demand creation for the broad base of customers and order fulfillment services.

All of our distributors stock inventory of our products. The distributors purchase products from us at a set distributor cost denominated in U.S. dollars. Title and risk of loss generally transfer upon shipment from our stocking locations, which are primarily located at the independent subcontractors we employ for test and assembly services in the Asia Pacific region or our warehouse in

San Jose. Upon shipment to the distributor, we generally defer revenue on the sale in accordance with our revenue recognition policy. Consequently, the deferred revenue and the corresponding deferred cost of sales are recorded as a current liability under the caption titled Deferred income and allowances on sales to distributors. All payments to us are denominated in U.S. dollars. For a detailed discussion of our revenue recognition policy, see Note 2 Significant Accounting Policies Revenue Recognition to our Consolidated Financial Statements.

Our sales cycle begins with a design-win phase, which is generally lengthy and often requires the ongoing participation of sales, engineering, and managerial personnel. Once customer demand has been created and a design is ready to move into prototyping or production, the order fulfillment process begins. Regardless of whether Altera, the independent sales representative, or the distributor created the demand, a local distributor will process and fulfill over 90% of all orders from customers. Our distributors are the legal sellers of the products and therefore bear all risks, such as credit loss, inventory shrinkage and theft, and foreign currency fluctuations that are generally related to the sale of commercial goods.

In accordance with our distribution agreements and industry practice, we have granted our distributors the contractual right to return certain amounts of unsold product on a periodic basis and also to receive price concessions for unsold product in the case

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of a subsequent decrease in list prices. We also provide price concessions to our distributors for a portion of their original purchase price in order for them to address individual negotiations involving high-volume or competitive situations. Typically, a customer purchasing a small quantity of product for prototyping or development from a distributor will pay list price. However, a customer using our products in volume production, purchasing thousands or even hundreds of thousands of units, will often competitively negotiate a substantial price discount from the distributor. Under such circumstances, the distributor will often negotiate and receive a price concession from Altera. In recent years, such concessions have exceeded 50% of list price on average. This is a standard practice in the semiconductor industry and we provide some level of price concession to every distributor.

Total sales is the sum of our own direct sales to original equipment manufacturers, or OEMs, and our distributors resales of Altera products. For the fiscal year ended December 30, 2005, worldwide sales through distributors for subsequent resale to OEMs, or their subcontract manufacturers, accounted for 93% of total sales. Arrow Electronics, Inc. is our largest distributor and on a worldwide basis accounted for 44% of total sales in 2005, 46% of total sales in 2004, 51% of total sales in 2003. Altima Corporation, which serves the Japanese market, accounted for 17% of total sales in 2005, 16% of total sales in 2004, and 16% of total sales in 2003. Paltek Corporation, which also serves the Japanese market, accounted for 10% of total sales in 2004, and less than 10% of total sales in 2005 and 2003. In March 2006, we terminated our distribution relationship with Paltek Corporation.

For a discussion of the risk factors associated with our distribution model, see Item 1A: Risk Factors *We rely heavily on distributors to generate a significant portion of our sales and fulfill our customer orders. The failure of our distributors to perform as expected would materially reduce our future sales* and *Conditions outside the control of our independent subcontractors and distributors may impact their business operations and thereby adversely interrupt our manufacturing and sales processes*. See also Note 2 - Significant Accounting Policies - Concentrations of Credit Risk to our Consolidated Financial Statements.

Altera Sales, Marketing, and Customer Support

Altera also maintains a dedicated global sales and marketing organization to create customer demand and manage the network of distributors and independent sales representatives. In general, Altera focuses its direct demand creation efforts on a limited number of key accounts, as well as providing technical, business, and marketing support to distributors and independent sales representatives. Independent sales representatives are mostly located in North America and in select European countries. Independent sales representatives create demand and provide customer support in a defined territory and, in many cases, with a defined set of customers. They stock no inventory and provide no order fulfillment services. All of our contracts with independent sales representatives may be terminated by either party in a relatively short period of time.

Customer support and service are important aspects of selling and marketing our products. We provide several levels of technical user support, including applications assistance, design services, and customer training. Also, we publish data sheets and application notes, conduct technical seminars, and provide design assistance via the Internet and electronic links to the customer.

Throughout the United States, we have domestic sales offices in numerous major metropolitan areas. In addition, we maintain international sales support offices in various metropolitan areas including Bangalore, Beijing, Cork, Helsinki, Hong Kong, London, Munich, Osaka, Ottawa, Paris, Seoul, Shanghai, Shenzhen, Singapore, Stockholm, Taipei, Tokyo, and Turin.

No single end customer accounted for more than 10% of our total sales in 2005, 2004, or 2003.

INTERNATIONAL SALES

International sales, which consist of all sales outside of North America, constituted 75% of total sales in 2005, 71% of total sales in 2004, and 67% of total sales in 2003. Sales to Japan accounted for 25% of total sales in 2005 and 2004, and 24% in 2003. Except for the United States and Japan, no other country accounted for sales in excess of 10% of total sales during 2005, 2004, or 2003. We expect international sales to continue to increase as a percentage of our total sales in the future. All of our sales to foreign entities are denominated in United States dollars. For a detailed description of our sales by geographic region, see Item 7: Results of Operations Sales by Geography and Note 11 - Segment and Geographic Information to our Consolidated Financial Statements. For a discussion of the risk factors associated with our foreign operations, see Item 1A: Risk Factors *Because we depend on international sales for a majority of our total sales, we may be subject to political, economic and other conditions that could increase our operating expenses and disrupt our business* and *Our business is subject to tax risks associated with being a multinational corporation.*

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Backlog

Our backlog consists mostly of distributor orders, as well as limited OEM orders, that are for delivery within the next three months. Our backlog of orders on December 30, 2005, was approximately $522.7 million, compared to $330.8 million on December 31, 2004.

Historically, backlog has been a poor predictor of future customer demand. While our backlog can increase during periods of high demand and supply constraints, purchasers may generally cancel product orders up to 30 days prior to the scheduled delivery date without incurring significant cancellation penalties. Further, we generally defer recognition of revenue on shipments to distributors until the product is resold. For all of these reasons, backlog as of any particular date should not be used as a predictor of future sales.

Manufacturing

Wafer Supply

Die, cut from silicon wafers, are the essential components of all our devices and a significant portion of the total device cost. Our manufacturing strategy is known as a fabless business model since we do not directly manufacture our silicon wafers. Instead, our silicon wafers are produced by independent semiconductor foundries. This enables us to take advantage of these suppliers high-volume economies of scale and also gives us direct and timely access to advanced process technology. We purchase nearly all of our silicon wafers from Taiwan Semiconductor Manufacturing Company, or TSMC, an independent semiconductor foundry. We have no formalized long-term supply or allocation commitments from TSMC. In the past, we have used other foundry vendors, and we may establish additional foundry relationships as they become economically beneficial or technically necessary. For a discussion of risk factors associated with our wafer supply arrangements, see Item 1A: Risk Factors *We depend entirely on independent subcontractors to supply us with finished silicon wafers. The failure of these subcontractors to satisfy our demand could materially disrupt our business,* *Shortages of, and/or increased costs for, our silicon wafers could lower our gross margins, reduce our sales, or otherwise materially disrupt our business,* *The manufacture of our products is complex, and the foundries on which we depend may not achieve the necessary yields or product reliability that our business requires,* and *Conditions outside the control of our independent subcontractors and distributors may impact their business operations and thereby adversely interrupt our manufacturing and sales processes*.

Testing and Assembly

After wafer manufacturing is completed, each silicon wafer is tested using a variety of test and handling equipment. The vast majority of our silicon wafer testing is performed at TSMC, and our San Jose pilot line facility, which is used primarily for new product development. This testing is performed on equipment owned by us and consigned to our partners.

The wafers are then shipped to various assembly suppliers in Asia, where good die are separated into individual chips that are then encapsulated in packages. We employ a number of independent suppliers for assembly purposes. This enables us to take advantage of these subcontractors high-volume economies of scale and supply flexibility, and gives us direct and timely access to

advanced packaging technology. We purchase almost all of our assembly services from Amkor Electronics, Inc., in Korea and the Philippines, and Advanced Semiconductor Engineering, Inc., or ASE, in Malaysia and Taiwan.

Following assembly, each of the packaged units receives final testing, marking, and inspection prior to being packaged for storage as finished goods. We obtain almost all of our final test and back-end operation services from Amkor and ASE. Final testing by these assembly suppliers is accomplished through the use of our proprietary test software operating on hardware that is consigned to or owned by our suppliers.

The majority of our inventory, including finished goods, is warehoused at our subcontract test and assembly partners located in Asia with a smaller portion located at our corporate facility in San Jose, California. On our behalf, these suppliers also ship our products to OEMs and distributors.

For a discussion of risk factors associated with our testing and assembly arrangements, see Item 1A: Risk Factors *We depend on independent subcontractors, located in Asia, to assemble, test, and ship our semiconductor products. The failure of these subcontractors to satisfy our demand could materially disrupt our business* and *Conditions outside the control of our independent subcontractors and distributors may impact their business operations and thereby adversely interrupt our manufacturing and sales processes*.

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Executive Officers of the Registrant

Our executive officers and their ages as of March 14, 2006 are as follows:

Name	Age	Position
John P. Daane	42	Chairman, President and Chief Executive Officer
Denis M. Berlan	56	Executive Vice President and Chief Operating Officer
John R. Fitzhenry	56	Vice President, Human Resources